LOW-POWER OP-AMP OPERATING IN SUB-THRESHOLD REGION WITH IMPROVED SLEW RATE

A Thesis submitted in partial fulfillment of the Requirements for the degree of

Master of Technology
In
Electronics and Communication Engineering
Specialization: VLSI Design & Embedded System

By
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Rourkela, Odisha, 769 008, India
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Dedicated to...

My Dear Friends

DEPT. OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA

ROURKELA – 769008, ODISHA, INDIA

CERTIFICATE

This is to certify that the work in the thesis entitled **Low-Power Op-Amp Operating In Sub-threshold Region with Improved Slew Rate** by **Apurbaranjan Panda** is a record of an original research work carried out by him during 2013 - 14 under my supervision and guidance in partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSI Design & Embedded System. Neither this thesis nor any part of it, to the best of my knowledge, has been submitted for any degree or diploma elsewhere.

Place: **Prof. M. N. Islam**

Date: Dept. of Electronics and Communication Engg.

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I certify that

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b) The work has not been submitted to any other Institute for any degree or diploma.

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Apurbaranjan Panda

30th May 2014

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APURBARANJAN PANDA

ABSTRACT

This thesis focuses on the weak inversion design of low power low voltage Op-amp. The main objective of this thesis is to improve the slew rate of the Op-amp with a very less amount of power consumption. For this purpose, an adaptive bias circuit is used to improve the slew rate of an Op-amp in sub-threshold region by increasing the drain current of the input stage transistor of Op-amp under the dynamic condition instead increasing the quiescent current to reduce the power consumption. In this thesis we present sub-threshold Op-amp circuit with two different adaptive bias topology. First, an adaptive biased circuit with WTA (Winner Take All) topology, which is used in a class A Op-amp circuit and this circuit designed using UMC 180nm technology with a supply voltage of 0.8V. The second one is an adaptive bias circuit based on current subtractor topology, this topology is used in a class AB Op-amp circuit with supply voltage of $\pm 0.6\,\mathrm{V}$. This thesis presents the comparison between Op-amp with adaptive bias (both topology) and without adaptive bias circuit.

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1

INTRODUCTION

1.1 Motivation

The operational amplifier (Op-amp) is a really significant and widely used building block in the analog and mixed signal circuit design field. The performance of Op-amp in the integrated circuit is affects overall performance of the system. Proper design of Op-amp is necessary according to the application requirement. The growing demand of portable electronics devices makes the circuit designer think about low power low voltage integrated circuit design. The tendency of bringing down the supply potential is a usual tactic to lower the power consumption in digital circuit. Whereas, the supply reduction subjects a number of challenges in the analog circuit design. As the technology shrinks the transistor length scales down, power supply scales down, but the scaling rate of the threshold voltage is not the same. Thus, the circuit behavior is obsoleted. Hence the design of Op-amp has become an essential feature in order to provide efficient benefits by technology scaling.

Working at very low supply voltage for an Op-amp a number of techniques were developed such as MOSFTE Bulk-Driven technique, Floating Gate MOS, use of charge pumps, and transistor operating in sub-threshold region. In sub-threshold region MOSFET the current variation and transconductance is very similar as the Bipolar Junction Transistor, in this region the small signal model is alike as in the saturation operation. Current value reaches a lower level by sub-threshold design approaches, hence speed limiting factor for an Op-amp could be observed in sub-threshold region. But for some applications power consumption is vital factor rather than the speed. Applications like, in biomedical signals where the amplitude of the signal is varies in some mV to uV range and the frequency lies in some kHz range. Then sub-threshold operation can be utilize for such application.

1.2 Literature Review

- G. Palmisano et al, in 2001, [1] have defined a simple design process for two stage CMOS operational amplifier for integrated into an analog design-based CAD tool. They discussed about typical frequency compensation techniques for high gain bandwidth product.
- M. Alioto, in 2010, [2], presented a paper about the DC behavior of sub-threshold CMOS logic for ultralow power circuit design perspective. They provides an effective implementation of small signal as well as large signal model for subthreshold region operation of MOS transistor.
- A.J. Lopez-Martin,in 2005, [3], presented a paper describes about the methods to reach low-voltage operational amplifiers with reduced power. In this paper he presented three OTA structure with three different types of adaptive biasing circuit. And all these three technique are implemented using the concept of level shifter based adaptive biasing technique.
- M. R. Valero et al. [4] presented a paper describes about low-power class-AB Op-amp design. All transistors used in this design of Op-amp are biased in subthreshold region. For improving the CMRR and slew rate of Op-amp common mode feed-forward path and adaptive biased technique are employed respectively.

- H. Fathabadi, in 2013, [5] presented a paper on a low voltage and ultra-low power operational transconductance amplifier (OTA). A current subtractor circuit is used as adaptive biasing to improve the transient response of Op-amp.
- David J. Comer et al.in 2004 [6], presented a paper based on the advantage of weak inversion operation of transistor used in the differential stage to get higher gain, less distraction and ease of compensation.
- Luca Magneelli et al., in 2012, [7], have proposed the procedure of systematic design of an Op-amp operating in the weak inversion region. And they found that Op-amp in subthreshold region gives highest value of FOM for power and load capacitor.

1.3 Overview of Thesis

This thesis presented a comparison study of low power Op-amp working in the sub-threshold region with the conventional CMOS Op-amp working in saturation. This thesis emphases the improvement of slew rate of sub-threshold Op-amp along with low power consumption. The basics of Op-amp and a conventional Op-amp simulation result is provided in Chapter 2 of the thesis. Chapter 3 describes about the sub-threshold behavior of transistor and simulation of an Op-amp operating in the sub-threshold region is carried. This chapter discussed about the problems appears in the sub-threshold Op-amp. Chapter 4 presents the solution to the problem occurred during the subthreshold operation of Op-amp. In this chapter two new Op-amp structure with adaptive biased circuit are presented for improving the slew rate of Op-amp. And also in this chapter we present comparison between all the Op-amp circuits presented in this thesis. The conclusions are drawn in chapter 5.

2

BASICS OF OP-AMP

Op-amp plays a vital role in analog and mixed signal circuit. It becomes one of ingenious building blocks in analog circuit design. It was designed by John R. Ragazzini in 1947 to represent a unique type of amplifier that, by appropriate selection of its external components. It could be organized in a collection of action, such as addition, subtraction, integration, differentiation and amplification. The first application of Op-amp was in analog computer [8]. Op-amps are the amplifiers that have sufficiently high forward open loop gain, so that when op-amps are used in negative feedback, the overall close loop transfer function becomes independent upon the forward path gain of the op-amp. This principle has been used to develop many useful analog circuits. The primary requirement of an op-amp is to have a very high open loop gain to implement the negative feedback concept, very high resistance at the input and low impedance at the output stage. Now a day the CMOS Op-amp circuits are frequently used in Integrated circuits. A two stage unbuffered CMOS Op-amp is very popular among all design technique. This thesis focuses mainly on various two stage unbuffered CMOS Op-amp design techniques.

2.1 Basics of Op-amp

Basically, in an Op-amp the input signal is a differential signal which is applied to a differential amplifier as the input stage and the output stage is a single ended output, which amplifies the difference of the two input given at the input stage of the Op-amp, hence there is a differential to single ended conversion circuit must present in an Op-amp circuit. As the output impedance of the Op-amp is very low and requires a high output voltage swing a buffered stage is used at the output. To achieve close loop stability a compensation circuit is required. The Figure 2-1 shows the basic block diagram of an Op-amp.

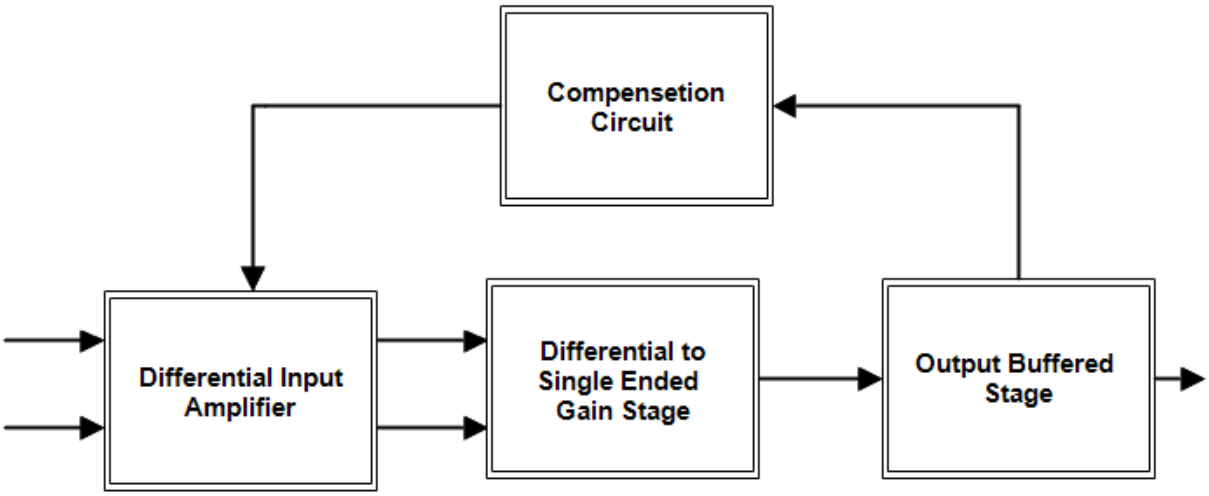

Figure 2-1 Basic Block Diagram of Op-amp

The differential amplifier is the input stage of the Op-amp. As its name suggests it processes the difference between the two input signals. It terminates the common mode voltage applied at the input terminals. As, it cancels most of the common voltage at the input, hence, noise and bias voltages are negated out. Most of the electronic circuits use differential amplifiers. But, practically some amount of common mode voltage factor is always exists at the output of the differential amplifier [8].

The output of the differential amplifier is stated as:

$$\boldsymbol{V_{out} = A_d(V_{in}^{+} - V_{in}^{-}) + A_C\left((V_{in}^{+} + V_{in}^{-})/2\right)}$$

Ideally,

$$\boldsymbol{A_C = 0}$$

Where $\boldsymbol{A_C}$ is the common mode gain of the amplifier and $\boldsymbol{A_d}$ is the differential mode gain of the amplifier.

By using a differential amplifier it is possible to cancel out noise and bias voltages that seem on both inputs so a small common-mode gain is typically considered decent. The common-mode rejection ratio is simply the ratio between differential-mode and common-mode gain and it symbolizes the efficiency of the amplifier in rejecting voltages that are

common to both inputs from affecting the output. Common-mode rejection ratio (CMRR) is given by:

$$CMRR = \frac{A_d}{A_c}$$

For an ideal differential amplifier A_c should be zero and CMRR should be infinite.

The differential amplifier used in CMOS technology gives a single ended output [9]. The out stage of two stage CMOS Op-amp is a common source which gives one more gain stage in cascade with the differential gain stage. For design an Op-amp with very low output impedance a source follower output stage is used which is treated as buffer stage.The compensation circuit is improves the phase margin of the system and the system becomes more stable. The desirable range of phage margin for a system is 45° to 60° [10].

2.2 Different Parameters Of Op-Amp

The performance of an Op-amp depends on the parameters associated with it, the parameters are given as below:

DC Gain: it is the open loop gain of the Op-amp. Ideally DC gain of an Op-amp is infinite, practically it is 60 dB to 100 dB

ICMR: It is defined as the range of common mode input voltage up to which the transistors associated with the differential stage (first stage) are in saturation and gives a constant gain.

CMRR: It is the ratio of differential mode gain to the common mode gain. An ideal Op-amp should have very high CMRR value, practically CMRR is more than 60 dB. It is one of the most important basic parameter of the Op-amp.

PSRR: The PSRR is defined as the product of ratio of the change in supply to change in output voltage of the amplifier cause by the change in the power supply and open loop gain of the Op-amp. It indicates how well the Op-amp doings to the deviation of power supply

(both positive and negative supply). Less is the variation of output of Op-amp corresponding to the variation of power supply, higher is the PSRR. An Op-amp should have very high PSRR. Practically this value is greater than 60 dB.

Slew Rate: It is defined as the maximum rate of change of output voltage w.r.to time. It is expressed in terms of V/us. A good Op-amp should have high slew rate. It determines by the charging and discharging of output capacitor by current available. Slew rate is completely depends on the current sourcing or sinking capability of the input stage rather than the output.

Settling time: It is the minimum time taken by the system to reach the steady state. For a typical OP-amp this value is less than 1us.

Phase Margin: It is defined as the excess of phase required to make the system marginally stable at the unit gain frequency. It is a measure of stability for close loop system.

PM = 180+ ϕ

ϕ = Phase of system when gain is 0 dB.

Practically for a well-designed Op-amp this value is around 60°.

For a becoming a system stable the phase margin and gain margin both are need to be positive. However, the consideration of a phase margin is very vital because it affects the transient response such as the settling time, slew rate, rise time, fall time and overshoot.

Input Offset Voltage: It defined as the voltage that must be applied between the two input terminals of an Op-amp to null or zero the output voltage.

2.3 Ideal and Practical values of different Op Amp parameters

Here Table 1 shows the comparison of different Practical and Ideal parameters of an OP-amp. Achieving ideal values of parameters for an Op Amp is very difficult with real life constraints.

Table 1: Comparison between Ideal and Practical parameters of Op-amp

IDEALLY	**PRACTICALLY**
R_{IN} = infinite	R_{IN} is very high (in terms of MΩ)
R_{OUT}=zero	R_{OUT} is a low value (in terms of KΩ)
DC GAIN = infinite	DC GAIN ≥ 60dB
BANDWIDTH =infinite	BANDWITH is very high value (in terms of MHz)
CMRR = infinite	CMRR ≥ 60dB
PSRR = infinite	PSRR ≥ 60dB
OFFSET = zero	OFFSET ≠ zero (in order of millivolts)
SLEW RATE = infinite	SLEW RATE ≥ 5 V/us

2.4 Different test circuits

For finding different characteristics parameter of an Op-amp various test circuit are employed. This section presents schematic configuration of different test circuit are used in this work.

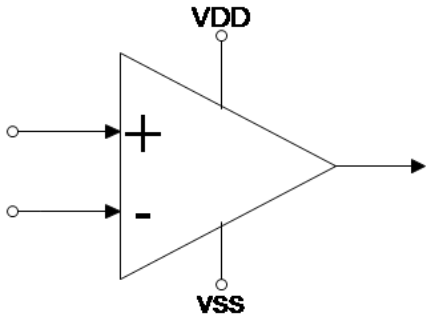

Figure 2-2 Symbol of OP-AMP [8]

The Figure 2-2 shows a simple symbolic representation of a linear 3-terminal Op-amp. Two input terminal are used for applying differential input signals into the Op-amp, the negative signed input is known as inverting terminal of the input and positive one is the non-inverting terminal. The Op-amp gives a single ended output and the output terminal is shown in the symbol as out pin. The pin V_{DD} and V_{SS} are shown in the symbol generally used as the terminals for the supply voltages. The op-amp is a dual power supplies component in which the V_{DD} terminal is used for positive power supply and V_{SS} is used for negative power supply, for some cases ground signal applied at the V_{SS} terminal.

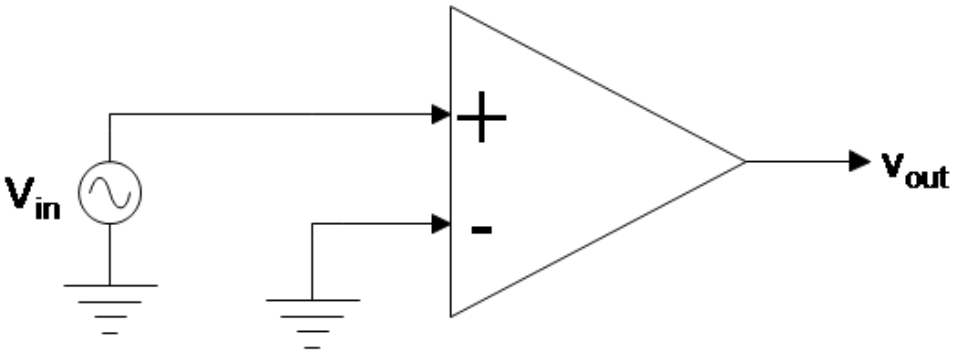

Figure 2-3 Test Circuit for Open-Loop Gain [10]

The Figure 2-3 shows the configuration for finding the open-loop gain of the Op-amp. Here an AC signal V_{IN} is applied to the non-inverting terminal and AC ground signal is applied to the inverting terminal with supply voltage of V_{DD} and V_{SS} an AC analysis is carried out. Then taking the ratio of output and input we can find the open-loop gain or DC

gain. By this configuration we can find out the UGB, phase margin and 3dB Band Width of Op-amp too.

$$DC\ Gain = \frac{V_{out}}{V_{in}} \tag{1}$$

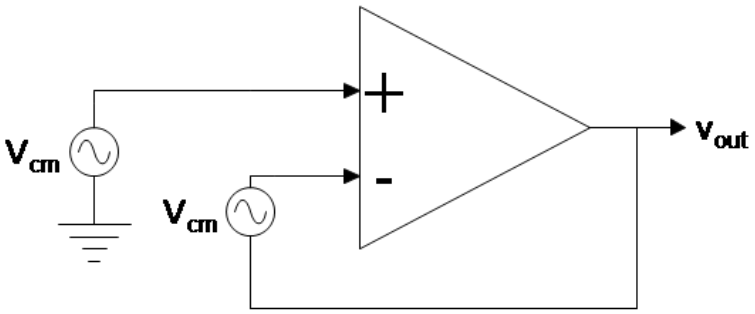

Figure 2-4 Test Circuit for CMRR [10]

The Figure 2-4 shows a simple configuration of finding the CMRR of an Op-amp. In this case in a unit gain configuration of Op-amp two identical ac signal source V_{cm} are connected in series with the inputs. An AC analysis is carried out for finding the CMRR of the Op-amp. CMRR is found by the Equ.(2) [10].

$$\frac{V_{out}}{V_{cm}} = \frac{1}{CMRR} \tag{2}$$

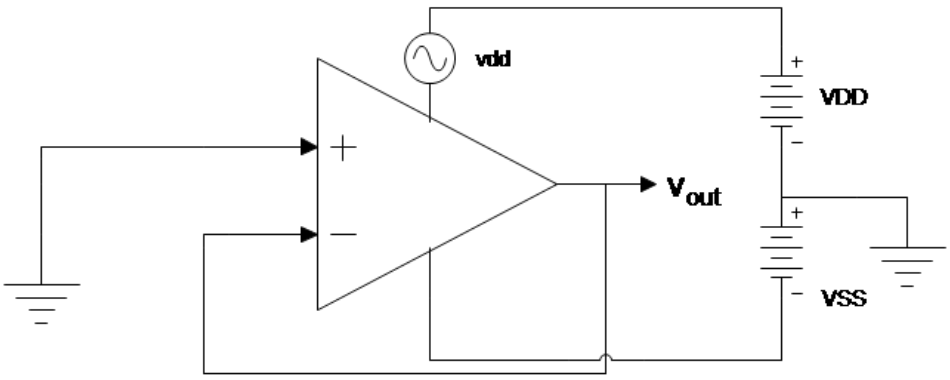

Figure 2-5 Test circuit for PSRR [10]

The Figure 2-5 shows a configuration for finding out the PSRR of an Op-amp. In this test circuit an ac signal vdd is connected in series with V_{DD} to measure the PSRR. By an AC analysis we can find out the PSRR of the Op-amp by the Equ. (3) [10].

$$PSRR = \frac{vdd}{V_{out}} \tag{3}$$

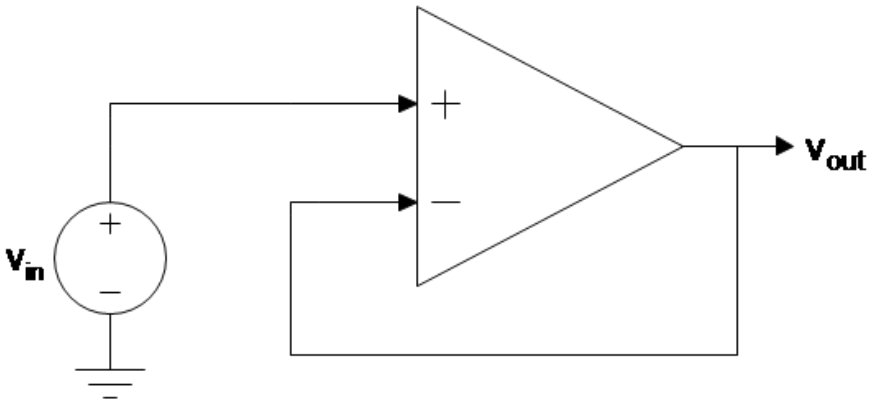

Figure 2-6 Test Circuit for Slew Rate [10]

The configuration shown in the Figure 2-6 is a simple diagram of unit gain configuration. This figure is used to find the slew rate and settling time of Op-amp by applying a step signal at non inverting input of the Op-amp. Observing output waveform of the Op-amp after a transient analysis we can find the SR and the settling time. From the slope of the output signal during rise or fall time of output waveform we can determine the SR.

2.5 Conventional CMOS Op-amp

A conventional two stage cmos Op-amp is shown in the Figure 2-7. The first stage of this Op-amp is consist of M1-M5 and M8 transistors, the second stage is consist of M6-M7 transistors and miller compensation capacitor C_C is used between the output and input of the second stage. All transistors used in this conventional Op-amp are operates in saturation region. The first stage is a differential stage, the differential signal is applied into the pin V_{in}^- and V_{in}^+ the gate terminals of the transistor M1 and M2 respectively. These transistor M1 and M2 are two NMOS driver transistors used to convert the differential voltage to differential current, these differential currents are given to the current mirrored

load transistor M3 and M4. The transistor M5 and M8 are used to provide the biasing current to the differential stage. The output of the differential stage is a single ended output signal and it gives the difference of the input signals with a constant gain. The second stage is a common source gain stage, the output of the first stage is applied to the gate of the M6 the transistor M7 is provides the bias current to the second stage and the output is taken from the drain terminal of the M6 [10].

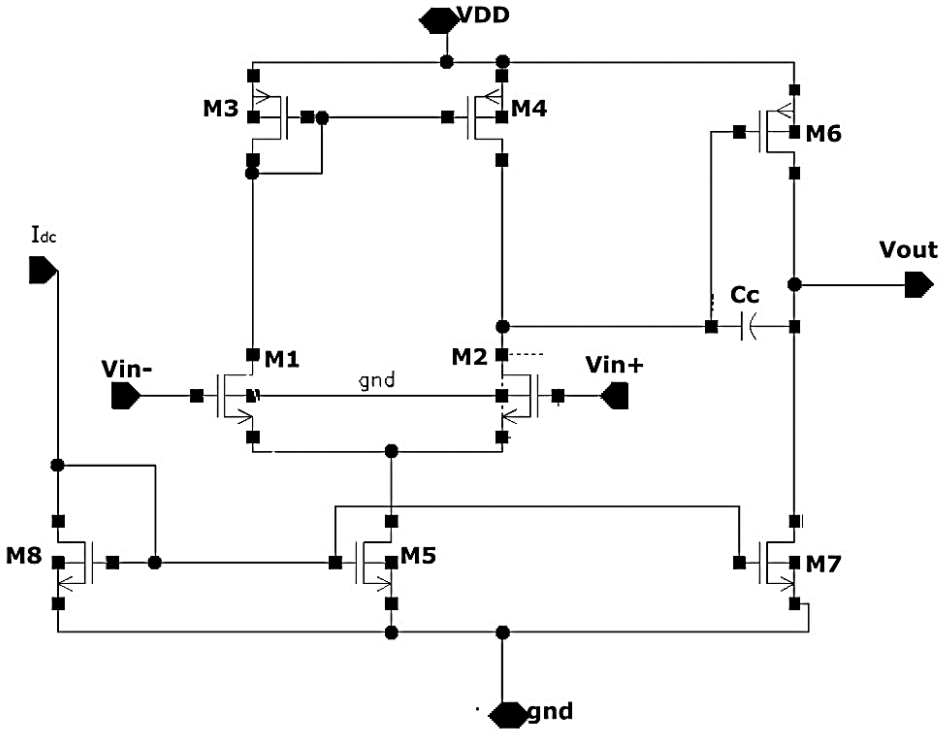

Figure 2-7 Conventional CMOS Two Stage OP-AMP

The DC gain of the first stage is

$$A_1 = -\frac{g_{m2}}{g_{ds2} + g_{ds4}}$$

The DC gain of the second stage is

$$A_2 = -\frac{g_{m6}}{g_{ds6} + g_{ds7}}$$

Overall gain of the Op-amp is [10]

$$A_V = A_1 . A_2$$

$$A_V = \frac{g_{m1} g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})} \quad (4)$$

Slew rate of the conventional Op-amp is [9]

$$SR = \frac{I_5}{C_C} \quad (5)$$

Where I_5 is the current through the M5 transistor and it is the bias current of the input stage.

The Gain bandwidth of the Op-amp is [9]

$$GB = \frac{g_{m1}}{C_c} \quad (6)$$

2.6 Simulation Results of Conventional Op-Amp

The conventional CMOS Op-amp shown in the Figure 2-7 is designed in UMC 180 nm technology with supply voltage of 1.8 V and a bias current I_{DC} of 20 uA. The simulation of this Op-amp is done by CADENCE spectre circuit simulator.

The gain and the phase plot of the conventional Op-amp circuit is shown in the Figure 2-8. This graph is plotted by simulating the Op-amp configuration shown in Figure 2-7. Here we applied a sinusoidal input signal of 10uV at a frequency of 1 KHz at the non-inverting input of Op-amp. We found 64.37dB DC gain, 64.19° phase margin, 25.55 MHz of UGB and a 15.94 KHz of 3dB band width for the conventional Op-amp. The power consumption of the Op-amp found out from the transient analysis is 276.8 uW.

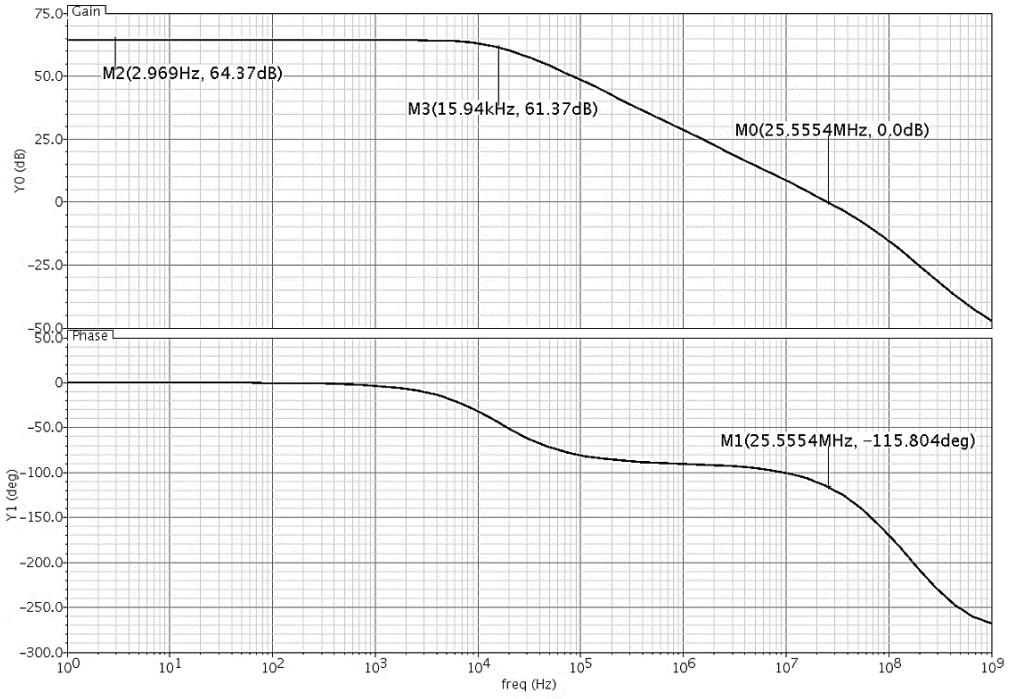

Figure 2-8 Gain and Phase plot of conventional Op-amp

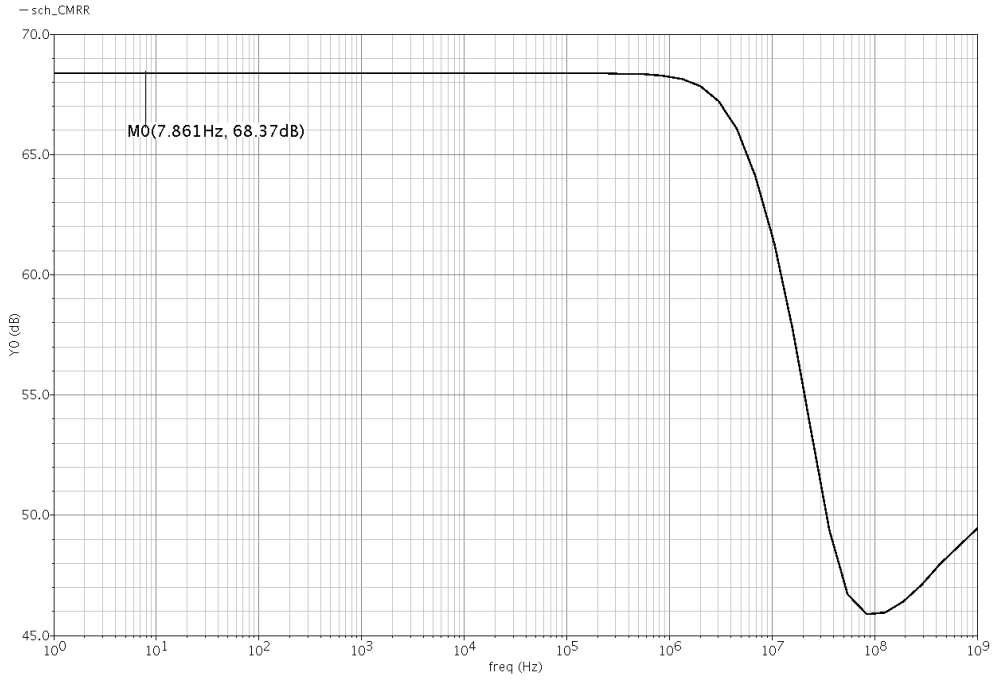

Figure 2-9 CMRR Plot of Conventional Op-amp

The waveform of CMRR of the conventional Op-amp is shown in the Figure 2-9 and the CMRR for this Op-amp 68.37dB. The PSRR of the Op-amp is 72.63dB shown in the Figure 2-10.

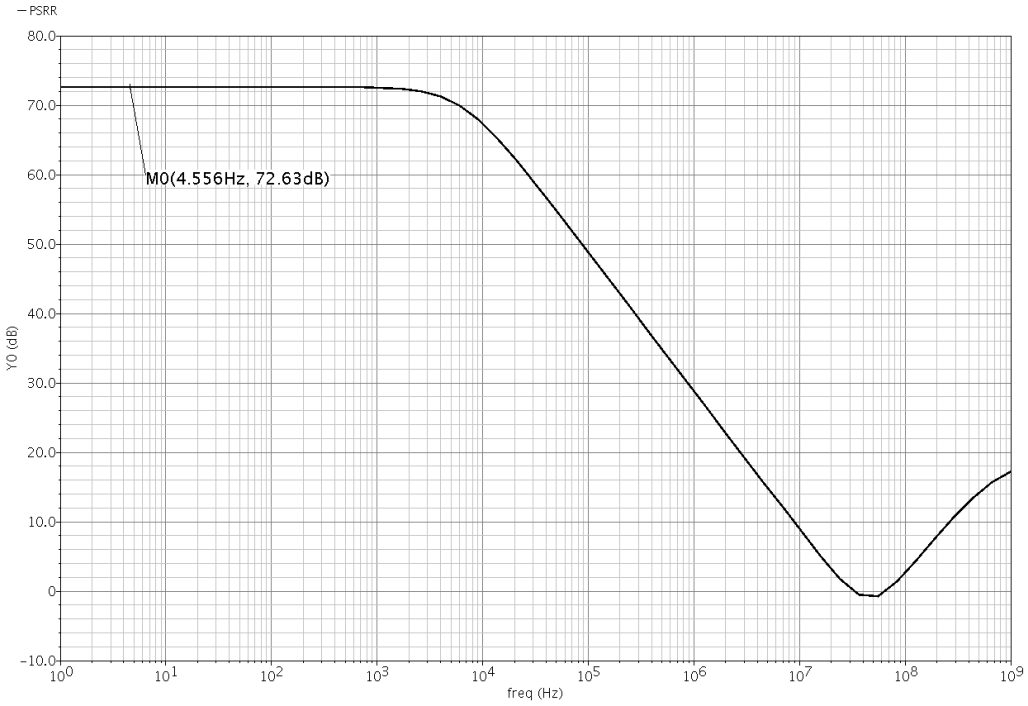

Figure 2-10 PSRR Plot of Conventional Op-amp

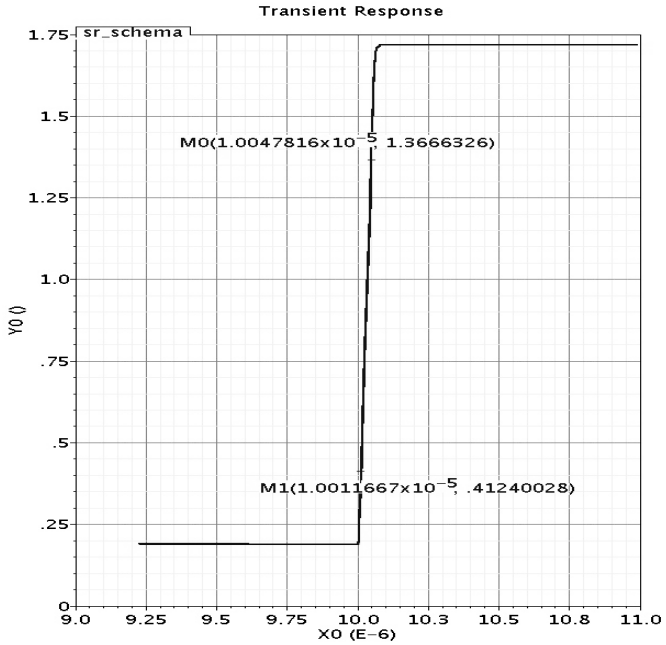

Figure 2-11 Slew Rate of Conventional Op-amp

Slew rate and settling time of the Op-amp is found from the Figure 2-11 is 26.4 V/us and 91.035ns respectively, for finding the SR a step signal increasing from 0V to 1.8V is applied at the non-inverting terminal of a unit gain configuration of Op-amp.

The layout of the conventional Op-amp is shown in the Figure 5-1 and the post layout simulation is done by CADENCE spectre layout simulator. The results of the post layout simulation is shown in Table 2.

Table 2: Simulation Results of Conventional Op-amp

Parameters	**Schematic simulation result**	**Post layout simulation Result**
DC Gain	64.37dB	64.39dB
CMRR	68.37dB	68.36dB
PSRR	72.63dB	72.65dB
UGB	25.55MHz	25.46MHz
SR	26.4V/us	26.3V/us
Phase margin	64.19°	66.63°
Settling time	91.035ns	98.614ns
Power	276.8uW	276.13uW

3

LOW POWER OP-AMP

With increasing the use of portable devices in medical science and wireless microsensor nodes like many other application. It is becomes a challenge to increase the life time of battery for those devices. Hence new circuit design technique needs to develop which consumes less power for increasing the battery life time. Then low power and low voltage circuit design is one alternate. As we know that Op-amp is a basic building block in the circuit design so power consumption of Op-amp need to be reduced. Power consumption can be decreases by reducing either total current in the circuit or supply voltage or by reducing the both. As we decrease input current, though power dissipation is lowered, but the dynamic range is affected and decreasing the supply voltage, it also becomes challenge to keep transistors in saturation region. The major drawback on implementing low-voltage CMOS circuits is the threshold voltage which does not scale down as the same rate as compared to the power supply [11]. From the previous chapter the CMOS Op-amp working in saturation region consumes power about 276.8uW. Transistor operating in sub threshold region in an analog circuit consume less energy for active operation and leakage power dissipation is less compare to the strong inversion region [7]. In the subthreshold region, the drain current I_D decreases but remains finite as V_{GS} drops several volt below V_T. The drain current reduces exponentially with V_{GS}. For low-voltage, low-power applications Sub-threshold operation of the MOSFET can be used If an Op-amp works in sub-threshold region the power consumption is less than working in saturation region.

3.1 Sub-threshold region operation of MOS transistor

Generally when a MOS transistor is operated in saturation region within any analog or digital circuit, we assumed that the transistor is off (drain to source current is zero) when the transistors gate to source potential is below threshold voltage of that transistor. But,

exactly below the threshold the drain current is exponentially proportional to the gate to source potential [12]. This current is known as “subthreshold current”.

The Figure 3-1 shows magnitude of inversion layer variation with gate to substrate voltage. In this region the inversion charge is exponentially varies with gate potential, but in strong inversion region the inversion charge linearly depends on gate potential this can be observed clearly in the Figure 3-2. The depletion region charge is a small quantity, because substrate of MOS transistor is a weakly doped region [13]. And in sub-threshold region the inversion charge is very less than the source to drain region. Only diffusion current flows in this region.

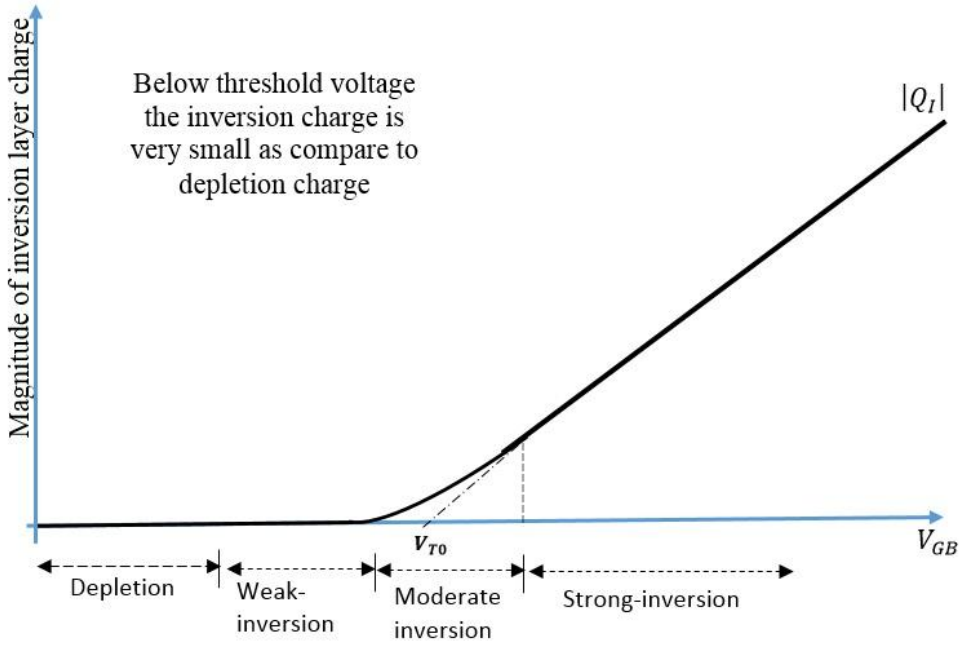

Figure 3-1 Magnitude of Inversion layer charge per unit area VS. Gate-Substrate Voltage [14]

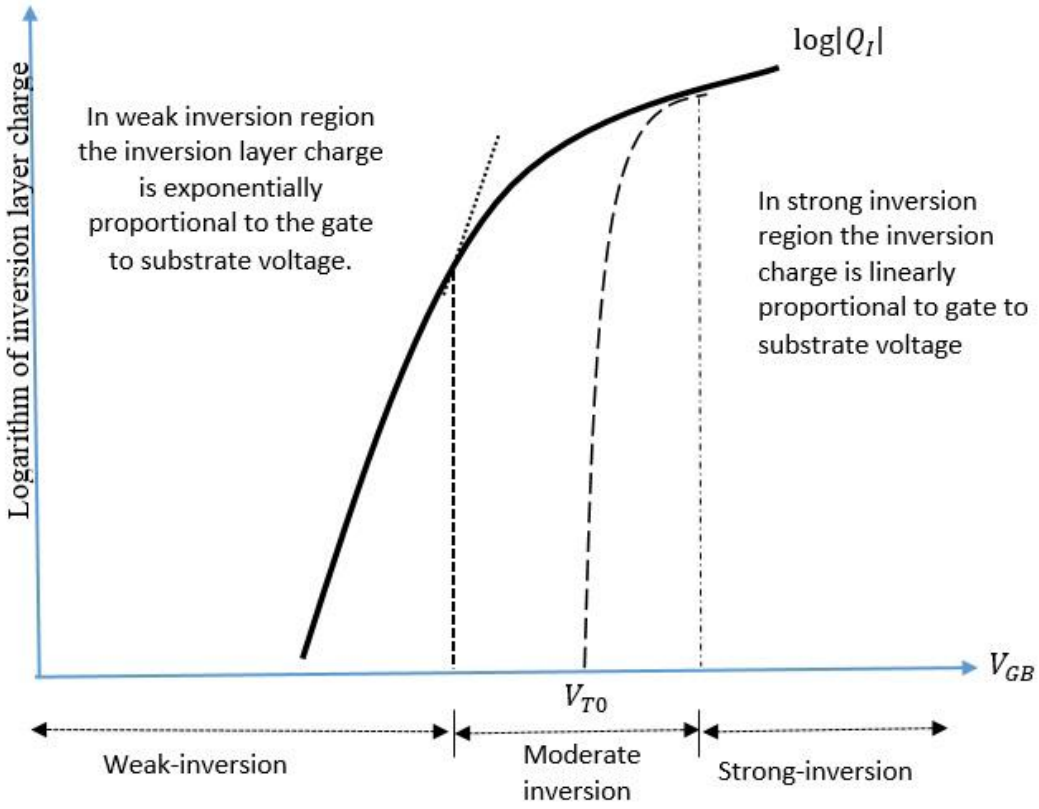

Figure 3-2 Logarithm of inversion layer charge per unit area VS. Gate substrate voltage [14]

3.1.1 Subthreshold current

In subthreshold region the drain current [7]

$$I_D = I_{spec}\, ex\, p\left(\frac{V_G - V_{TH0}}{nV_T}\right)\left[ex\, p\left(-\frac{V_S}{V_T}\right) - ex\, p\left(-\frac{V_D}{V_T}\right)\right] \quad (7)$$

$$I_D = I_{D0} exp\frac{V_G}{nV_T}\left(exp\frac{-V_S}{V_T} - exp\frac{-V_D}{V_T}\right) \quad (8)$$

Where

$$I_{D0} = I_{spec} exp\frac{-V_{TH0}}{nV_T} \quad (9)$$

Where

$$I_{spec} = 2n\mu C_{OX}\frac{W}{L}V_T^2 \quad (10)$$

Where n is the sub-threshold slope factor $\left(\mathrm{n} = 1 + \frac{\mathrm{C_d}}{\mathrm{C_{ox}}}\right)$ [14], V_{TH0} is the threshold voltage of the transistor, V_G is the gate voltage, V_S is the source voltage, V_D is the drain voltage, V_T is the thermal potential $[V_T = \frac{kT}{q}]$, k is Boltzmann constant, T room temperature in Kelvin [300K], q is charge of electron. C_{OX} is the oxide capacitance and μ is mobility of electron.

If $V_{DS} > 4V_T$, then $exp\frac{-V_{DS}}{V_T} << 1$, since $e^{-4} \cong 0.018$. The last term in Equ. (7) is approaches equal to one, which can be ignored. The expression for drain current then simplifies to:

$$I_D = I_{spec} exp \frac{V_{GS} - V_{TH0}}{nV_T} \qquad (\text{saturation } V_{DS} > 4V_T) \qquad (11)$$

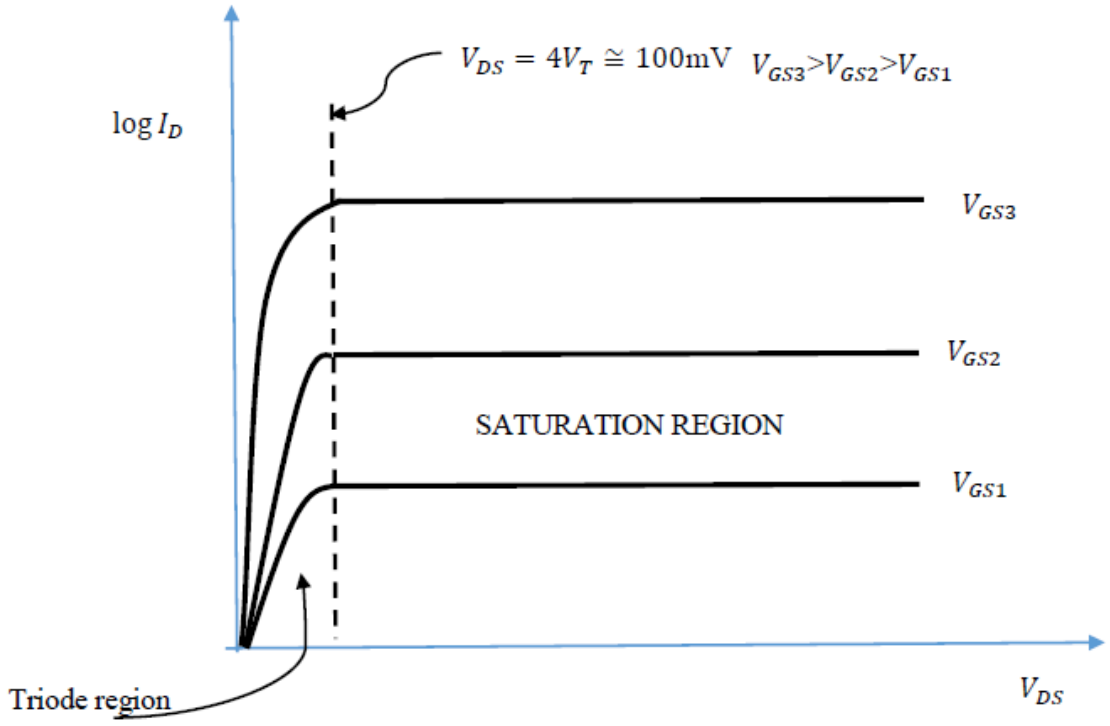

Figure 3-3 Output characteristics of an n-channel MOSFET operating in the sub-threshold region in a log-linear plot [13]

The above Equ. (11) is independent on the value of V_{DS}, hence when $V_{DS} > 4V_T$ in the sub-threshold region, this region can be treated as saturation of MOSFET in sub-threshold.

As V_{DS} required to do so and it does not depend on V_{GS} as in the case above threshold. It is easy to keep the MOSFET in saturation for subthreshold operation. This is very beneficial for low-voltage designs.

Figure 3-3 shows that when $V_{DS} = 4V_T \cong 100\text{mV}$ the drain current saturated but in triode region the drain current increases with increase inV_{DS}.

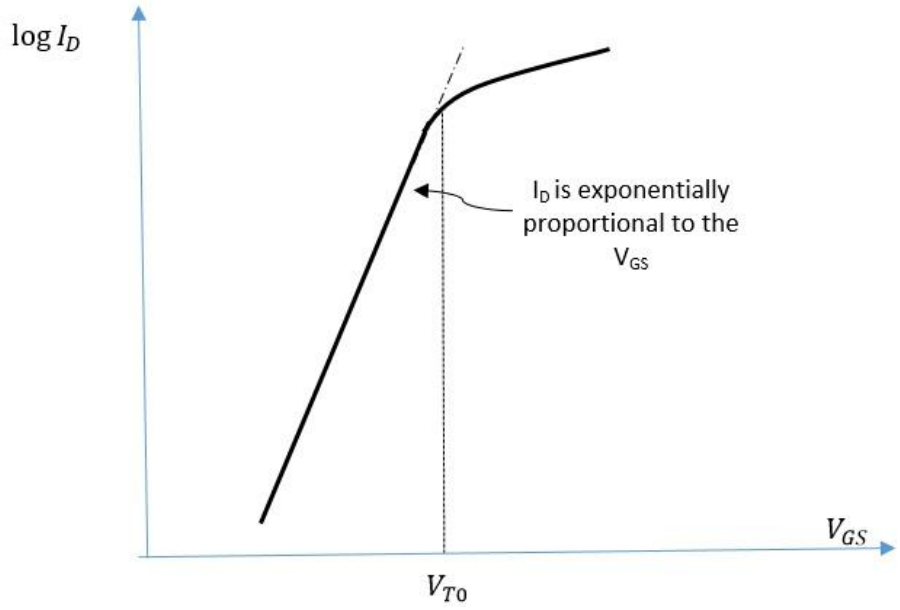

Figure 3-4 Drain Current Verses Gate Source Potential of A MOSFET in Saturation Region in Log Scale [13]

The changes occurs in drain current as the gate to source voltage changes creates the difference between above threshold and sub-threshold region operation of MOS transistor. The current increases exponentially in a weakly-inverted MOSFET. Whereas the current increases quadratircally (square law) in a strongly-inverted MOSFET. Figure 3-4 shows the plot for I_D with V_{GS} in logarithmic scale.

3.1.2 Transconductance of MOSFET in sub-threshold region

Transconductance of a subthreshold MOSFET is:

$$g_m = \frac{I_D}{nkT/q} \tag{12}$$

Equ. (12) shows a linear relationship between transconductance and drain current in sub-threshold region. And the transconductance is independent upon device geometry when the drain current constant. These two features of the sub-threshold region distinguish from the strong inversion region, where the relation between transconductance and drain current is a gives a square-law and also for the device geometry.

The subthreshold MOSFETs behaves very much like BJT transistor, both drain current and transconductance is very much similar as of BJT. A bipolar transistor has a transconductance of $g_m = \frac{I_D}{V_T}$, which is equivalent to the expression for a subthreshold MOSFET if we set n=1. For a MOS transistor current through its gate is zero, but in a bipolar transistor always there is a small amount of current pulls by its base. This can make circuit design much simpler.

3.1.3 Capacitance of MOSFET in sub-threshold region

Intrinsic capacitors present in a MOSFET are due to the charge stored in the channel. Each of these capacitors are dependent upon the fraction of the total gate oxide capacitor WLC_{OX} according to the bias voltage. The extrinsic capacitors are the source and drain junctions capacitors and the gate overlap capacitors to source and drain diffusions [13]. Their values are basically independent of the drain current.

In weak inversion, most of the intrinsic capacitor values are very small if the channel is small. The gate-to-substrate capacitance made by the series connection of C_{OX} and the depletion capacitance C_d is the only non-negligible capacitance .it is given by [13]:

$$C_{GB} = \frac{n-1}{n} WLC_{OX} \tag{13}$$

And is smaller than the WLC_{OX}(total gate oxide capacitance).

3.1.4 Leakage current in sub-threshold region

In saturation region the only dominating leakage current is due to the DIBL (Drain Induced Barrier Lowering) factor [13]. The effect of DIBL on I_D can be taken in to account on the V_{TH} expression as follows [2].

$$V_{TH} = V_{TH0} - \lambda_D V_{DS} - \lambda_B V_{BS} \quad (14)$$

The values of λ_D and$\lambda_B > 0$,

Where V_{BS} is the body to source voltage, λ_D is the DIBL effect compnent and λ_B is substrate effect component. The DIBL effect is associated to the distance between drain and source region i.e. the λ_D is mainly depends on L.

3.1.5 Small signal MOSFTE parameters in sub-threshold region

From the above discussion and equations the small signal parameters (transconductance g_m, drain to source resistance r_d, the substrate trance conductance g_{mb} and DC gain) of a transistor in the sub-threshold region are reported in the Table 3.

Table 3: Small signal MOSFET parameters in sub-threshold region

PARAMETERS	IN SUB-THRESHOLD REGION
$g_m = \frac{\partial I_D}{\partial V_{GS}}$	$\frac{I_D}{nV_T}$
$r_d = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1}$	$\frac{1}{\lambda_D I_D}$
$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$	$\frac{\lambda_B I_D}{nV_T}$
$A_{V0} = g_m r_d$	$\frac{1}{nV_T \lambda_D}$

3.2 Op-amp operating in Sub-threshold Region

In the chapter 2 we have seen that the conventional Op-amp is consume power in a range of hundreds of uW. The power of the Op-amp is depends upon the bias current of the input as well as the output stage. The bias current is the drain current of the transistor used for biasing. We have seen that the drain current of the transistor is touches a lower value when operates in sub-threshold region, the small signal model of Op-amp in sub-threshold is very similar that of the saturation region and $\frac{g_m}{I_D}$ value reaches the maximum value in this region [13] . Hence an Op-amp designed in sub-threshold region will consume less power as compared to the saturation region operation.

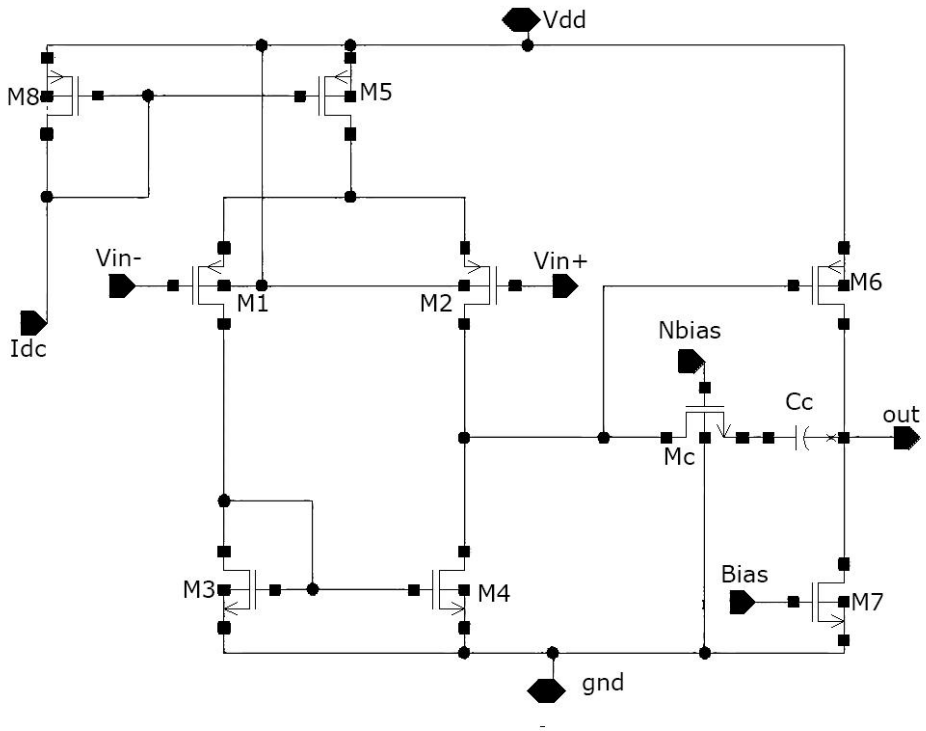

Figure 3-5 Two Stage Op-amp Operating in Sub-threshold Region

The Op-amp shown in the Figure 3-5 is a two stage Op-amp configuration operating in the sub-threshold region where PMOS transistors are used as the input of the differential

stage. Because the $1/f$ noise is five time less in PMOS transistor than NMOS transistor [10]. All the transistors are used in this Op-amp are operates in the weak inversion region. The transistor M1- M5 and M8 are the first stage and M6-M7 are used as the second stage of the Op-amp. Where M1 and M2 are the driver transistor which converts the differential input to differential current, M3 and M4 are forms current mirrored load to convert the differential current to single ended output voltage and the transistor M5 gives the bias current to input stage and the capacitor Rc and the transistor M_C makes a frequency compensation network for achieving close-loop stability of the Op-amp. The transistor M_C is used instead of the resistor required for the RC compensation network.

The DC gain of the Op-amp shown in the Figure 3-5 is very similar to the DC gain is conventional Op-amp

$$\mathrm{A_V} = g_{m2}(R_{O2}||R_{O4})g_{m6}(R_{O6}||R_{O7})$$

The value of the R_O is the output resistance of the transistor

$$R_O = \frac{1}{\lambda I_D}$$

Then

$$A_V = \frac{g_{m2}}{\mathrm{I_{D2}}\lambda_2 + \mathrm{I_{D2}}\lambda_4}\frac{g_{m6}}{\mathrm{I_{D6}}\lambda_6 + \mathrm{I_{D7}}\lambda_7}$$

$$A_V = \frac{1}{n_2 n_6 V_T^2(\lambda_2 + \lambda_4)(\lambda_6 + \lambda_7)} \quad (15)$$

The (15) shows that the gain of the Op-amp in sub-threshold region is depends on the values of λ and the sub-threshold slope factor. The sub-threshold slope factor for the transistor is a constant ($1 < n < 2$). As λ depends upon the channel length, L is the only design parameter to set the gain of the Op-amp in the sub-threshold region. The bias

current of the differential pair can be set by the required input referred noise spectral density [7]. The g_m of the input stage transistor also fixed with fixing the bias current.

The gain-bandwidth product (GBW) of the Op-amp is

$$GBW = \frac{I_{D1}}{2\pi n_1 V_T C_C}$$

And

$$GBW = \frac{g_{m1}}{2\pi C_C} \tag{16}$$

The slew rate of the Op-amp is

$$SR = \frac{I_{D5}}{C_C} = \frac{2I_{D1}}{C_C}$$

$$SR = 2.GBW.n_1 V_T \tag{17}$$

From the (15) it is seen that the DC gain of the sub-threshold Op-amp is independent upon the drain current it is only depends upon value of L whereas the SR and GBW of the Op-amp is dependents upon the value of the drain current. Hence the SR of the Op-amp is reduced while operating in sub-threshold region.

The design of Op-amp in sub threshold region for specific parameters is carried out as follows [7]:

From the specified value of DC gain we can set the value of L for transistor used in the Op-amp.

For achieving essential input referred noise power spectral density the bias current of the differential stage can set

$$I_{D1,2} = \frac{4q\left(n_{1,2}V_T\right)^2}{S_{vw}}$$

Where S_{vw} is the white noise component which is generally available at the high frequency, for low frequency a gate referred flicker noise component is added to the inputs.

From (12) the transconductance of the first stage is automatically fix with fixing the value of $I_{D1,2}$. From the drain current equation the aspect ratio of the transistor M1,2 is set for a suitable V_{SG} value, which makes the transistor to work in weak inversion region.

$$\left(\frac{W}{L}\right)_{!,2} = \frac{I_{D1,2}}{2n\mu C_{OX} V_T^2} \exp\left(\frac{|V_{TH}| - V_{SG}}{n_{1,2} V_T}\right)$$

The compensation C_C can be set either from the value of GBW or from the value of SR. As the $g_{m1}$is fixed from the desire value of GBW we can find the value of C_C as follows

$$C_C = \frac{g_{m1}}{2\pi . GBW}$$

The bias current of the second stage is fixed for getting the maximum output swing in the output of the Op-amp. After the fixing the value of the bias current in the second stage we can set the value of aspect ratio of $M_{6,7}$ by using the drain current equation.

For setting the R_C (compensation resistance) for the RC compensation network we have to consider the load capacitance, parasitic capacitance at the output of first stage and the desired phase margin as for the design strategy given in [1]

$$R_C = \frac{1}{2g_{m7}}\left(1 + \sqrt{1 + \frac{4gm_7 C_L}{g_{m1} C_1 \tan(\phi_M)}}\right)$$

As in this Op-amp we replaced the resistor with transistor M_C, we can set the aspect ratio of the transistor and its gate potential for matching the $1/g_{ds}$of the transistor with the value of R_C found from the above equation.

3.3 Simulation Result

The simulation of the Op-amp schematic shown in the Figure 3-5 is carried out in CADENCE circuit simulator with a supply voltage of 0.8V and bias current of 140nA applied to the I_{DC} node. The Op-amp is designed in UMC 180nm technology and channel length of 720nm.

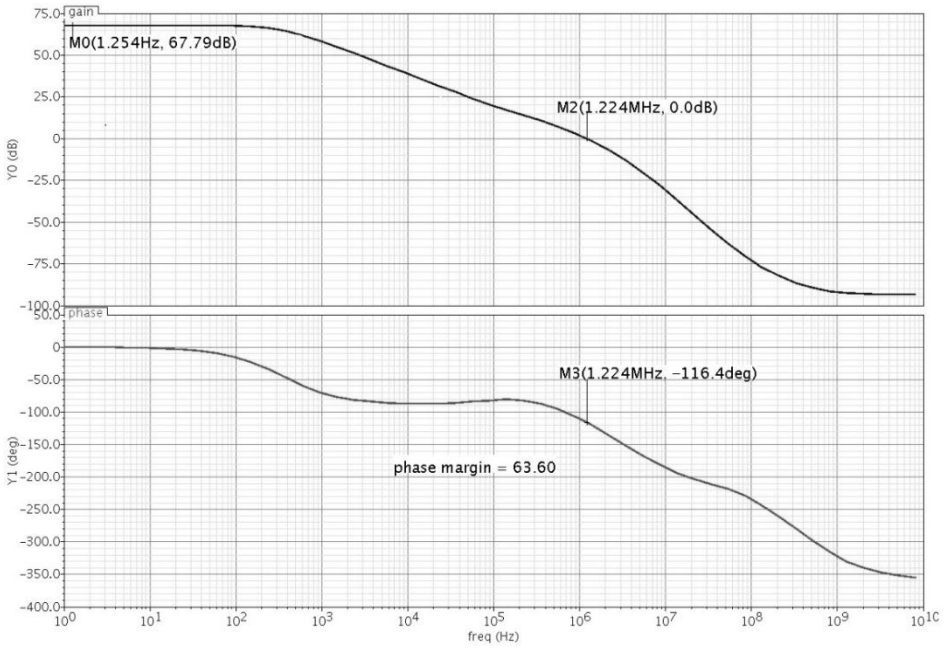

Figure 3-6 Gain and Phase Plot of Op-amp operating in subthreshold region

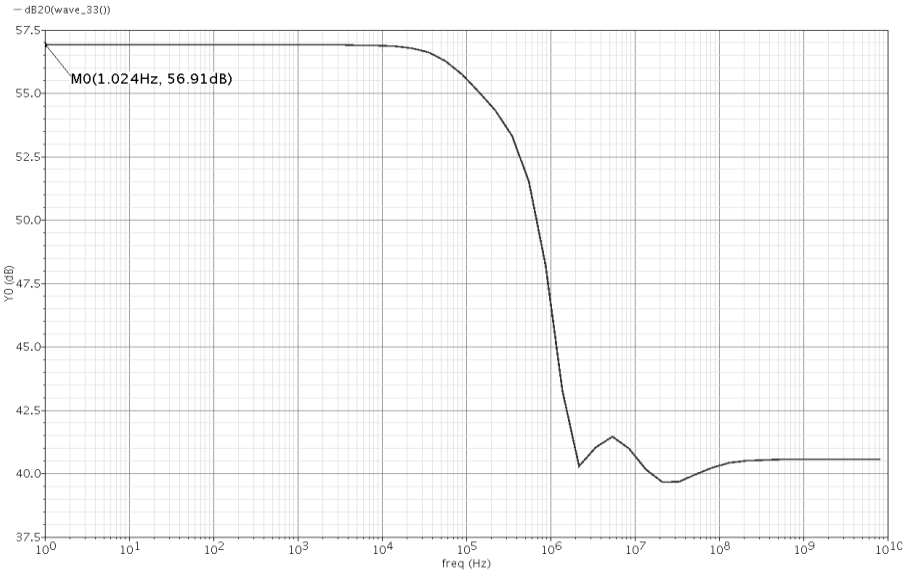

Figure 3-7 CMRR of the Op-amp operating in the subthreshold region

The Figure 3-6 is shows the gain and phase plot of the Op-amp described in the previous section, from this plot we have seen that the gain of the Op-amp is 67.79dB, UGB is 1.224MHz,3dB band width is 328.5KHz and phase margin is 63.6°. The power consumption of this circuit is found by the transient analysis is 830.48nW.

The Figure 3-7 is shows the CMRR plot of the Op-amp shown in the Figure 3-5, the CMRR of this Op-amp is 56.91dB. The PSRR of this Op-amp is found by using the test circuit shown in the Figure 2-5 is 34.51dB.

For finding the slew rate and the settling time of Op-amp we have applied a pulse signal of two voltage level 0 and 400mV, rise time and fall time of 1ns and the period the signal is 100us with pulse width of 50us to a unit gain configuration and the output of this configuration is shown in the Figure 3-8. The slew rate and the selling time of the Op-amp are 0.3116V/us and 5.28 us respectively.

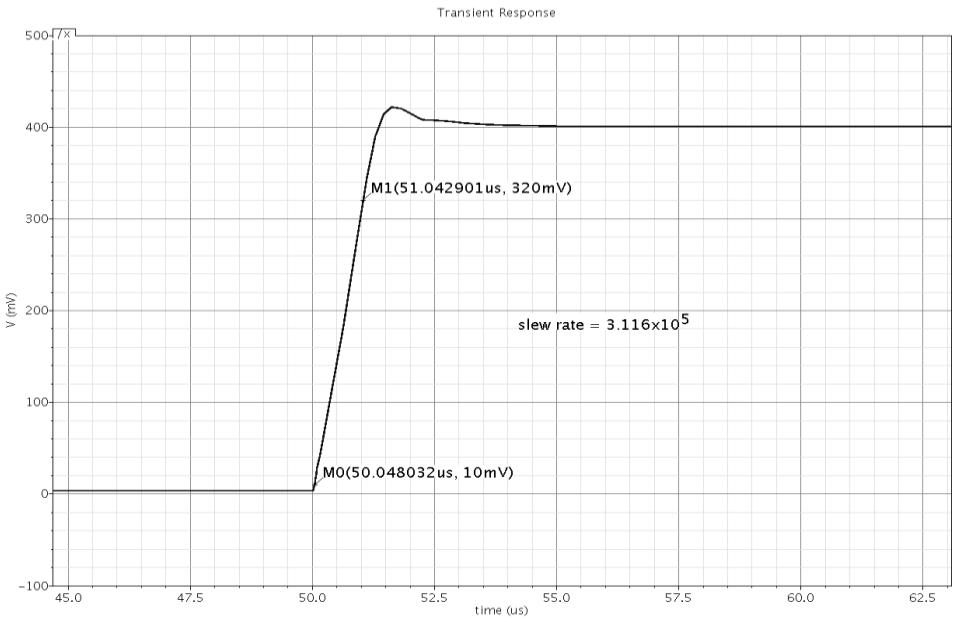

Figure 3-8 Slew Rate of Op-amp operates in subthreshold region

The layout of the Op-amp operating in sub-threshold region is shown in the Figure 5-2 and the post layout simulation is done by CADENCE spectre layout simulator. The results of the post layout simulation is shown in Table 4.

Table 4: Simulation Results of Op-amp operating in sub-threshold region

Parameters	**Schematic simulation result**	**Post layout simulation Result**
DC Gain	67.79dB	67.7dB
CMRR	56.91dB	57.62dB
PSRR	34.51dB	34.47dB
UGB	1.224MHz	1.183MHz
SR	0.311V/us	0.308V/us
Phase margin	63.60°	60.6°
Settling time	5.28us	5.41us
Power	830.48nW	830.51nW

4

SUB-THRESHOLD OP-AMP WITH IMPROVED SLEW RATE

A power efficient and high slew rate conventional Op-amp design in the sub - threshold region is quite difficult because the charging and discharging of the load capacitor depends upon the biased current of the input stage. And the slew rate of an Op-amp is always depends upon the bias current too. If the bias current somehow increased so that of total power of the amplifier is not permitted to increase then the slew rate limitation can be improved. An adaptive bias circuit used to remove the bias current limitation for a differential signal applied at the input stage. A block diagram of an Op-amp with adaptive bias circuit is presented in the Figure 4-1.As the adaptive bias circuit is used to increase the slew rate of Op-amp by increasing the biasing current under the dynamic condition without changing the quiescent current of the Op-amp gives the benefit of low power consumption.

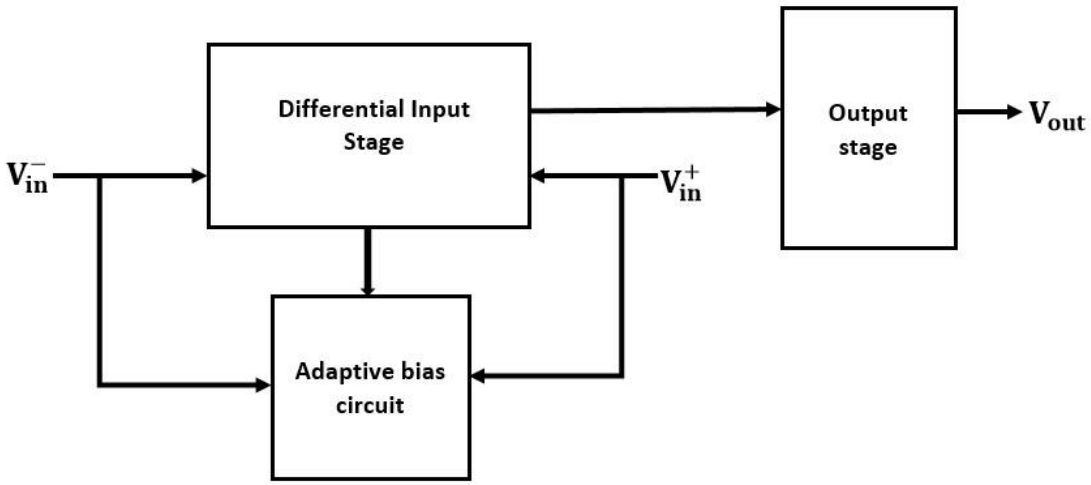

Figure 4-1 Simple Block Diagram of an OP-AMP with Adaptive Bias Circuit

4.1 Adaptive Bias circuit

The adaptive bias circuit is provided the bias current depending upon the difference of the input signal applied at the differential stage of the Op-amp. Various types of adaptive bias circuits are discussed in [15, 16, 4, 5] .

4.1.1 WTA Adaptive Bias Circuit

The WTA (winner takes all) circuit design is based on the adaptive biasing topology using two level shifter [3]. The adaptive biasing circuit using two level shifter is shown in the Figure 4-2. Here two driver stage transistor of an Op-amp is cross coupled by two DC level shifter.

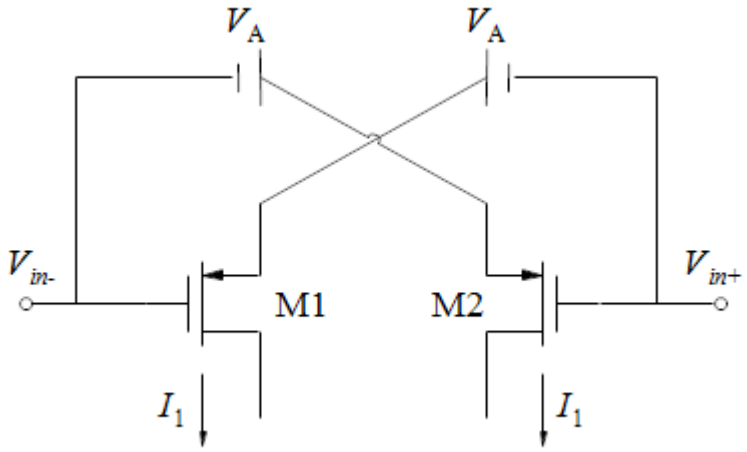

Figure 4-2 Adaptive bias circuit using level shifter [3]

When the gate to source voltage of both the transistor are equal i.e. $V_{SG1} = V_{SG2} = V_A$ (Quiescent condition). Then both the transistor M1 and M2 carry the same amount of DC current by V_A. If V_{in+}decreases the source potential of the M1 transistor is decreasing, but the voltage at the source of the M2 is remains unchanged. So the current through M1 decrease and the current through M2 increases. The current reaches the maximum value which is very high than the DC current under the quiescent condition. To drive the low impedance source terminals of M1 and M2 transistor very low impedance level shifters are required. And the level shifter circuit should have the capability to produce a large current during the charging and the discharging period of load capacitor.

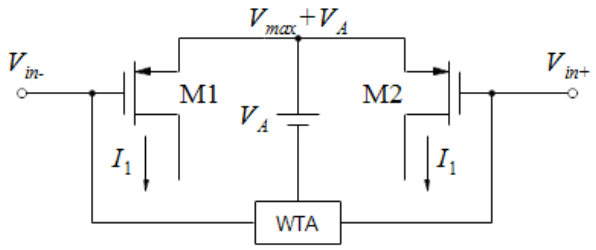

Figure 4-3 Adaptive bias topology using WTA Block [3]

The Figure 4-3 shows a diagram of adaptive bias topology using WTA Block, WTA block output is always the maximum or "winner" of the input voltages. The reflected at the common source node of M1 and M2 is a maximum of input voltages V_{max} shifted by the constant DC voltage V_A. When V_{in}^{+} and V_{in}^{-} are equal i.e. under quiescent condition the common source terminal gives maximum value relates the common mode voltage V_A of the input signals. Therefore $V_{SG1} = V_{SG2} = V_A$, and the quiescent currents through the driver transistors are depends and controlled by V_A in the similar way it works in the circuit shown in Figure 4-2.

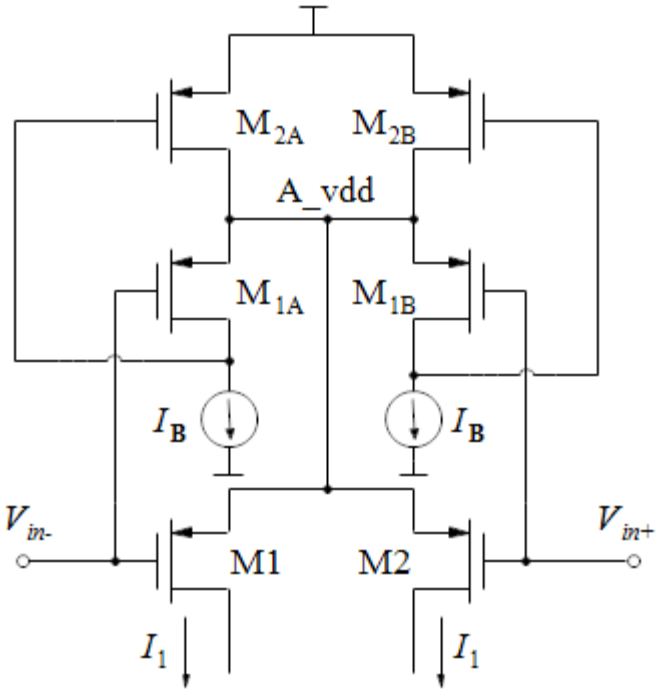

Figure 4-4 Circuit diagram of a WTA topology [3]

Under the dynamic condition when a difference occurs between the input signals, if the V_{in}^{+} decreases, that means it is lower than V_{in}^{-} then the common source terminal tracks higher input voltage i.e. V_{in}^{-} higher than the common mode voltage of the inputs. . Therefore, the resulting source to gate voltage $V_{SG2}$is larger than previous topology for the same input voltage, and a larger dynamic current boost up is attained.

The Figure 4-4 shows a circuit diagram of a WTA topology. Here for the transistor M1, M1A, M2 and M2B all the gate and source terminals are tied together. Under the quiescent condition when a common mode voltage is applied ($V_{in}^{+} = V_{in}^{-} = V_{cm}$) the voltage at A_vdd will be $V_X = V_{cm} + V_A = V_{cm} + V_{SG,1A-B}$, the current follows is the quiescent current I_B. When V_{in}^{-} decreases$V_{SG,1B}$ increases then the drain current of M1A transistor increases, so the drain voltage of M1A is also increasing. As the drain of the M1A is connected to the gate of M2A transistor the current through M2A decreases that reduces the potential at the node A_vdd, but on the other side the V_{in}^{+} increase that increases the node potential of A_vdd, Therefore the potential of A_vdd V_X is set by V_{in}^{+} , the aspect ratio of M1B and the current I_B, i.e. $V_X = V_{in}^{+} + V_{SG,1B}$. Similarly, when V_{in}^{+} decreases below V_{in}^{-} the node voltage of A_vdd becomes $V_X = V_{in}^{-} + V_{SG,1A}$.

$$I_B = I_{spec} \exp\left[\frac{V_{SG,1A,1B} - |V_{TH}|}{nV_T}\right] \tag{18}$$

For $V_{id} > 0\text{V}$, $V_{in}^{+} > V_{in}^{-}$, $V_X = V_{in}^{+} + V_{SG,1B}$ and currents I_1 and I_2 are

$$I_1 = I_{spec} \exp\left[\frac{-V_{in}^{-} + V_X - |V_{TH}|}{nV_T}\right] \tag{19}$$

$$I_1 = I_{spec} \exp\left[\frac{-V_{in}^{-} + V_{in}^{+} + V_{SG,1B} - |V_{TH}|}{nV_T}\right] \tag{20}$$

$$I_1 = I_{spec} \exp\left[\frac{V_{id} + V_{SG,1B} - |V_{TH}|}{nV_T}\right] \quad (21)$$

$$\frac{V_{SG,1A,1B} - |V_{TH}|}{nV_T} = \ln\left(\frac{I_B}{I_{spec}}\right) \quad (22)$$

Then

$$I_1 = I_{spec,1} \exp\left[\ln\left(\frac{I_B}{I_{spec}}\right) + \frac{V_{id}}{nV_T}\right] \quad (23)$$

$$I_1 = I_B \exp\left[\frac{V_{id}}{nV_T}\right] \quad (24)$$

And

$$I_2 = I_B \quad (25)$$

In a similar way, for $V_{id} < 0\text{V}$, $V_{in-} > V_{in+}$, $V_N = V_{in-} + V_{SG,1A}$ and currents I_1 and I_2 are

$$I_2 = I_{spec,2} \exp\left[\frac{-V_{in}^{+} + V_X - |V_{TH}|}{nV_T}\right] \quad (26)$$

$$I_2 = I_B \exp\left[\frac{-V_{id}}{nV_T}\right] \quad (27)$$

And

$$I_1 = I_B \quad (28)$$

Hence from the equation (7), (8), (10) and (11) we have seen that by using the WTA circuit the current through M1 and M2 increases exponentially with $|V_{id}|$ under the dynamic condition.

Hence

$I_1 = \max\left(I_B\, exp\left[\frac{V_{id}}{nV_T}\right], I_B\right)$ and $I_2 = \max\left(I_B\, exp\left[\frac{-V_{id}}{nV_T}\right], I_B\right)$

For a fully balance input ac signal the node A_vdd is an ac ground and $v_{gs,1,2} = \pm v_{id}/2$. The differential current for small signal condition is $i_d = i_1 - i_2 = g_{m1,2} v_{id}$ similar to the simple Op-amp structure because, due to use of WTA circuit the largest $V_{SG}$of the input transistors is $V_{SG,1A} + |V_{id}|$.

4.1.2 Op-amp with WTA circuit

We discussed about WTA topology in the previous section which can used as an adaptive bias circuit in an Op-amp circuit for improving the SR of the Op-amp by increasing the tail current under the dynamic condition.

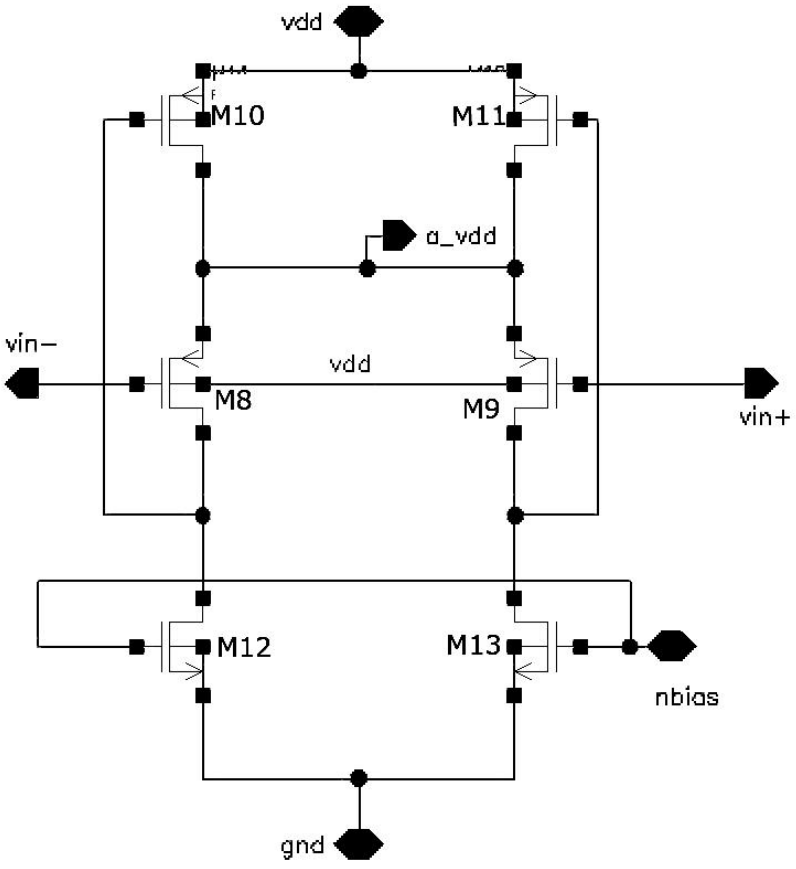

Figure 4-5 Schematic of WTA circuit

The Figure 4-5 shows the schematic of the WTA circuit the transistor M12 and M13 are used as the current source, which provides the bias current under the quiescent condition

for that these two transistor are operates in the saturation region. As we discussed the WTA circuit always tracks to the higher value of the input signal we can observe that from the plot shown in Figure 4-6.

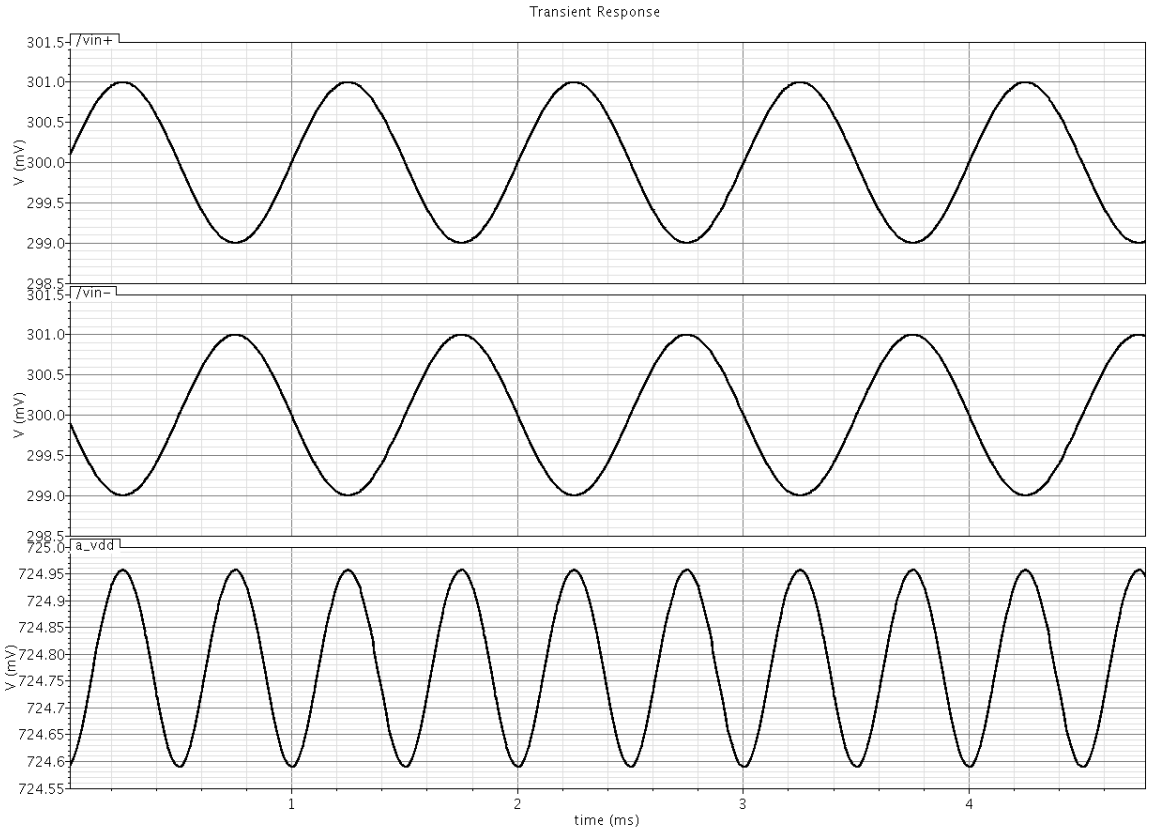

Figure 4-6 Simulation result of WTA circuit

Figure 4-6 shows the result of WTA circuit, when any one of the input signal V_{in}^{+} or V_{in}^{-} goes high the voltage at node a_vdd grasps maximum value and it gives minutest value when both inputs are the same.

The Figure 4-7 shows an Op-amp circuit without any bias current circuit, the configuration of this Op-amp is very similar to the Op-amp discussed in the section 3.2 but in this case the node a_vdd of this Op-amp is connected to a_vdd node of the WTA circuit, here the a_vdd node of WTA circuit is connected to the common source terminal of the driver transistor at the differential stage. The source and gate of the transistor M8 and M9 are connected with transistor M1 and M2 of the input stage of the Op-amp respectively.

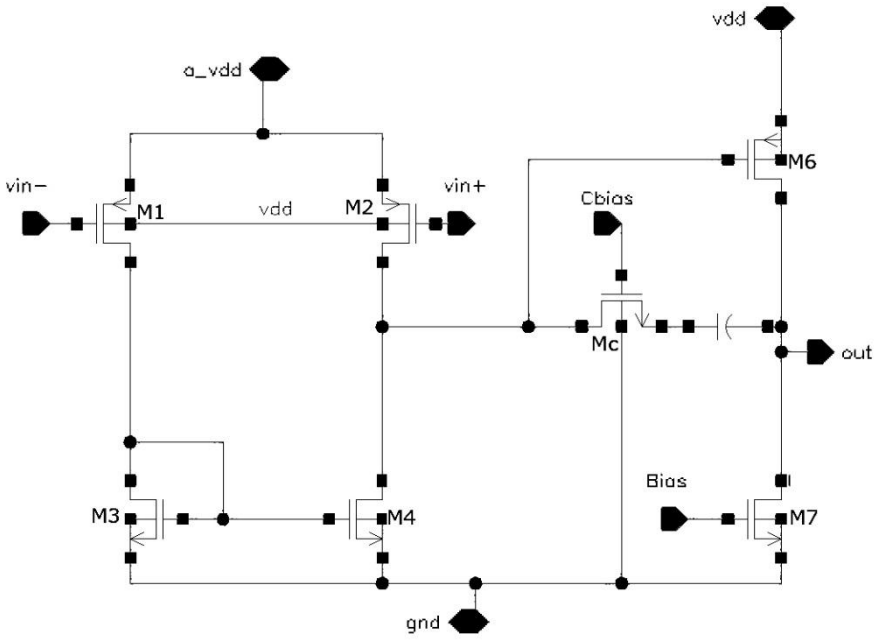

Figure 4-7 Schematic of Op-amp without current bias circuit

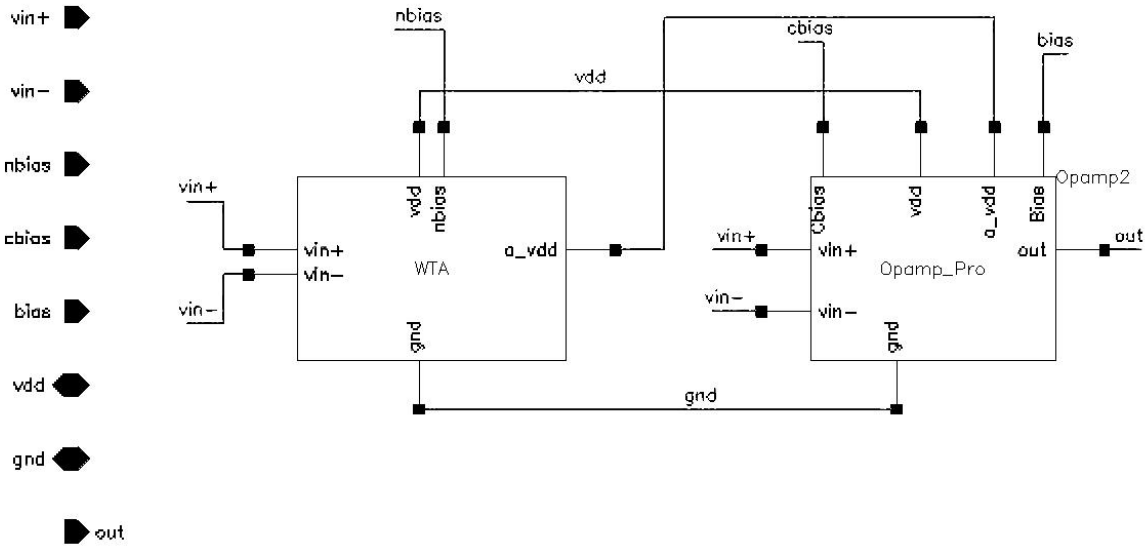

Figure 4-8 Op-amp with WTA circuit

The complete structure of Op-amp with WTA structure is shown in Figure 4-8. Here all the transistors are in sub-threshold region except M12 and M13. In this circuit three bias voltage supply (cbias, nbias and bias) required for operating the circuit properly. The "nbias" biased voltage node is connected to the M12 and M13 that makes these two transistor to work in saturation region as well as for providing the bias current to the

circuit. Through the node "cbias" a bias voltage is supplied to the transistor M_C that makes the transistor work as a compensating resistor, which is connected in series with the compensating capacitor for making a RC compensation network. The node "bias" is used to provide a biased current to the second stage of the Op-amp.

4.1.3 Simulation result for the Op-amp with WTA circuit

The design of the circuit shown in the Figure 4-8 is done by using the UMC 180nm technology with a supply voltage of 0.8V and the simulation of the circuit is carried out by using Cadence circuit simulator ADE (analog design environment).

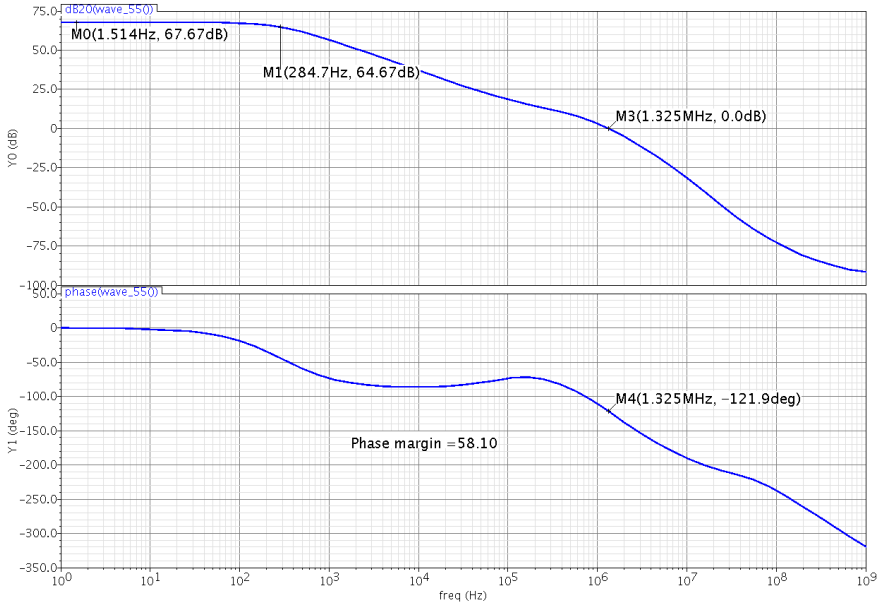

Figure 4-9 Gain and Phase plot of Op-amp with WTA circuit

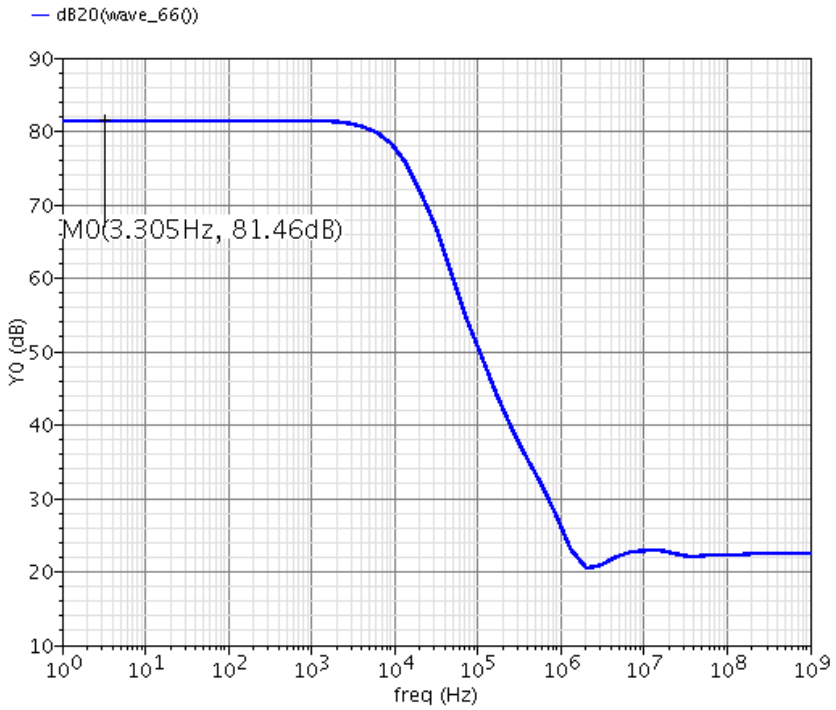

Figure 4-10 CMRR plot of Op-amp with WTA circuit

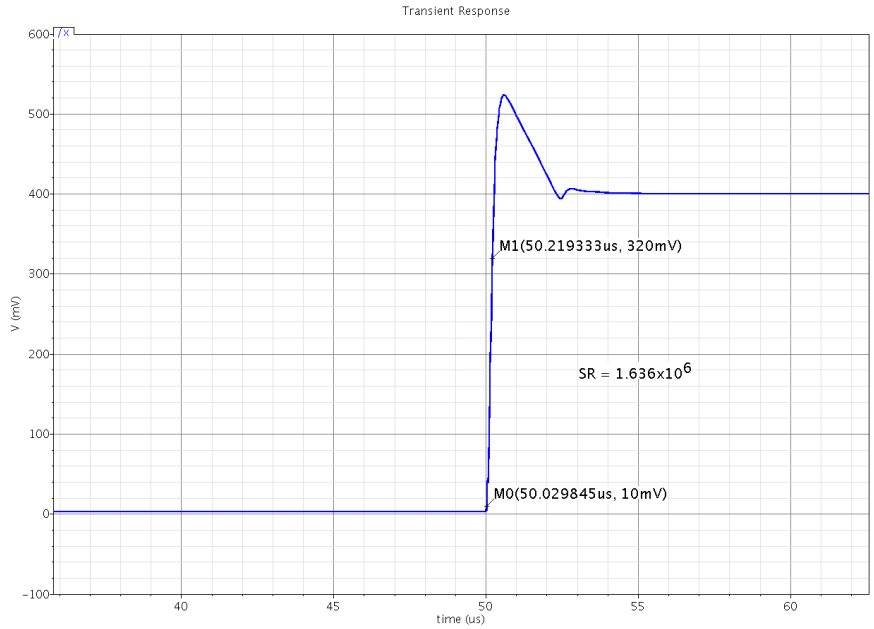

Figure 4-11 Slew rate of Op-amp with WTA circuit

The Figure 4-9 is shows the gain and phase plot of the Op-amp operating in sub-threshold region with adaptive bias circuit, from this plot we have seen that the gain of the Op-amp is 67.67dB, UGB is 1.325MHz, 3dB band width is 284.7 KHz and phase margin is

58.1°. The power consumption of this circuit is found by the transient analysis is 1.002uW.The Figure 4-10 is shows the CMRR plot of the Op-amp shown in the Figure 4-8, the CMRR of this Op-amp is 81.46dB. The PSRR of this Op-amp is found by using the test circuit shown in the Figure 2-5 is 34dB. For finding the slew rate and the settling time of Op-amp we have applied a pulse signal of two voltage level 0 and 400mVto a unit gain configuration and the output of this configuration is shown in the Figure 4-11. The slew rate and the selling time of the Op-amp are 1.69V/us and 4.6us.

The layout of the Op-amp operating in sub-threshold region is shown in the Figure 5-3 and the post layout simulation is done by CADENCE spectre layout simulator. The results of the post layout simulation is shown in Table 5

Table 5: Simulation Results of sub-threshold Op-amp with WTA adaptive bias circuit

Parameters	**Schematic simulation result**	**Post layout simulation Result**
DC Gain	67.67dB	67.66dB
CMRR	81.45dB	81.463dB
PSRR	34.0dB	33.9dB
UGB	1.325MHz	1.269MHz
SR	1.636V/us	1.695V/us
Phase margin	58.1°	55.0°
Settling time	4.66us	4.63us
Power	1.0027uW	1.0042uW

4.2 Adaptive bias circuit based on current subtractor topology

An adaptive biased circuit based on subtractor is circuit is presented in this section [5]. The Figure 4-12 shows the circuit diagram of the subtractor circuit.

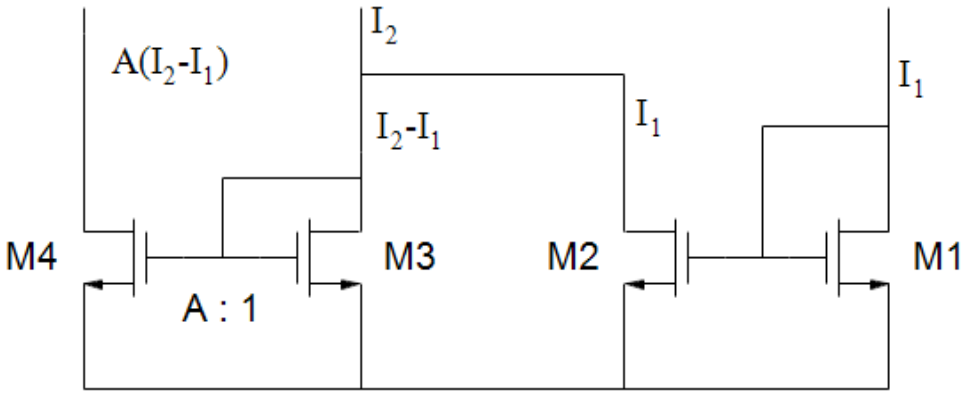

Figure 4-12 Current subtraction circuit [5]

The current I_1 and I_2 are related to the signal applied to the differential stage of the Op-amp. Here current I_1 flows through M1 and is mirrored by the M1 and M2 current mirror pair circuit. Current flows through M3 is $I_1 - I_2$ and the mirrored transistor M4 gives the current with a gain of A and the current at the M4 transistor becomes $A(I_1 - I_2)$.

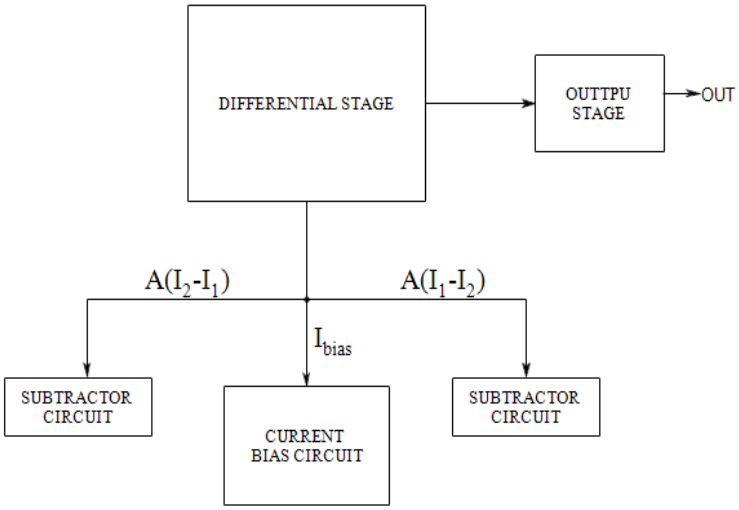

Figure 4-13 Block diagram of Op-amp with subtractor circuit

The Figure 4-13 shows a block diagram of an Op-amp with subtractor circuit as adaptive biased circuit. Two subtractor blocks are used to provide improvement in the bias current under the dynamic condition. This subtractor adaptive biasing circuit is generally used in a class AB output stage type Op-amp circuit.

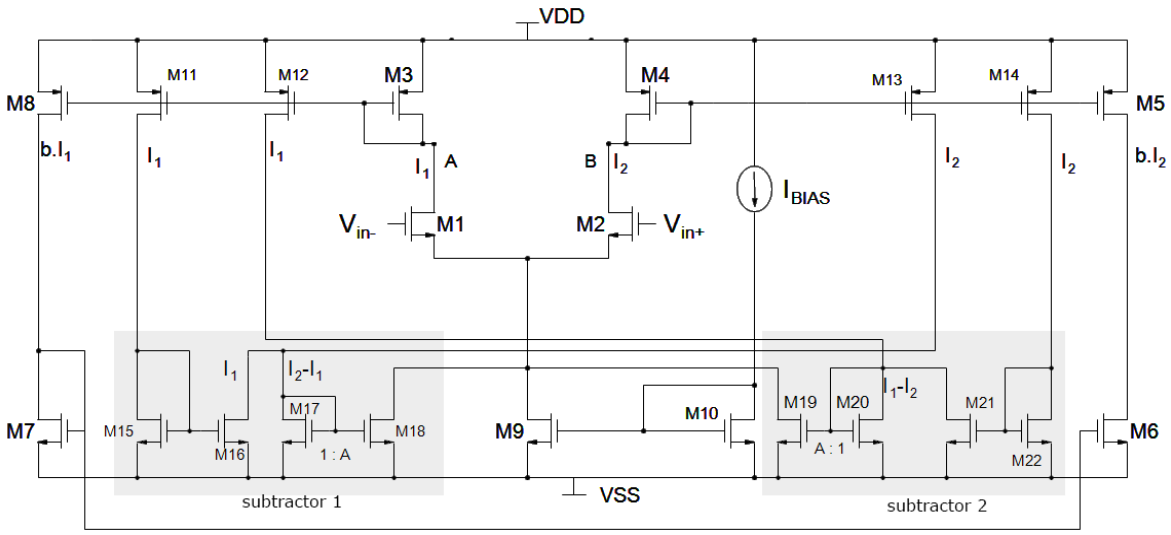

Figure 4-14 Two stage class AB Op-amp with subtractor circuit

The circuit diagram shown in Figure 4-14 is a simple class AB stage OTA (operational transconductance amplifier) with two subtractor circuit. The shaded region shows two subtractor circuit connected to solve the current limitation for improving the slew rate. The transistor M1-M10 are form a conventional OTA circuit, all other transistors are used for making current subtractor circuit.

1.1.1 Operation of current subtractor adaptive bias circuit

In the Figure 4-14 the current I_1 flows through M1 and M3 and this current is mirrored in M11, M12 and M16. The current I_2 flows through M2 and M4 and it is mirrored in M13, M14, and M21. I_{BIAS} current flows through M10 and mirrored in M9. The drain of M9 is connected to the common source terminal of the M1 and M2. Under the quiescent condition when differential signal is zero i.e. $V_{in+} = V_{in-}$ the tail current becomes I_{BIAS}. When differential voltage $V_d < 0$ i.e. $V_{in+} < V_{in-}$ then I_1 increases more than I_2. Hence maximum current flows through M1. The transistor M1, M3, M12, M20 and M19 creates a positive feedback loop that further increases the current through M1 and reduces the current through M2 and it becomes off. Therefore, I_2 becomes zero and I_1 increases to I_{BIAS}. The current I_1 is mirrored in M11, M16 and the current through M17 becomes

negative hence the transistor M17 and M18 becomes off. And current I_1 flows through M20 and the current through M19 will be $A.I_1$. As $I_1 = I_{BIAS}$ the tail current becomes

$$I_{tail} = I_{BIAS} + A.I_{BIAS}$$

Further this current returned and increased with gain of A through M1,M3 in the feedback loop created by M1, M3, M29, M20 and M19. Repetitively this course continues, hence the tail current becomes.

$$I_{tail} = I_{BIAS}(1 + A + A^2 + \cdots) = I_{tail} = I_{BIAS} \sum_{n=1}^{+\infty} A^n$$

Where A is the ratio of aspect ratio of M18,19 to M17,20

When A becomes greater than one the I_{tail} tends to infinity, therefore A must be less than 1. Then

$$I_{tail} = \frac{I_{BIAS}}{1 - A}$$

When A=0 this circuit is not behave like adaptive bias i.e. total tail current becomes I_{BIAS}. Hence we have to keep the aspect ratio of M18,19 always less than the aspect ratio of M17,20.

The first stage gain of OTA shown in the Figure 4-13 is $\frac{g_{m1}}{g_{m2}}$ a very small value which affect the overall gain of the amplifier. To increase the gain another gain enhanced network is added to the circuit as shown in the Figure 4-15.

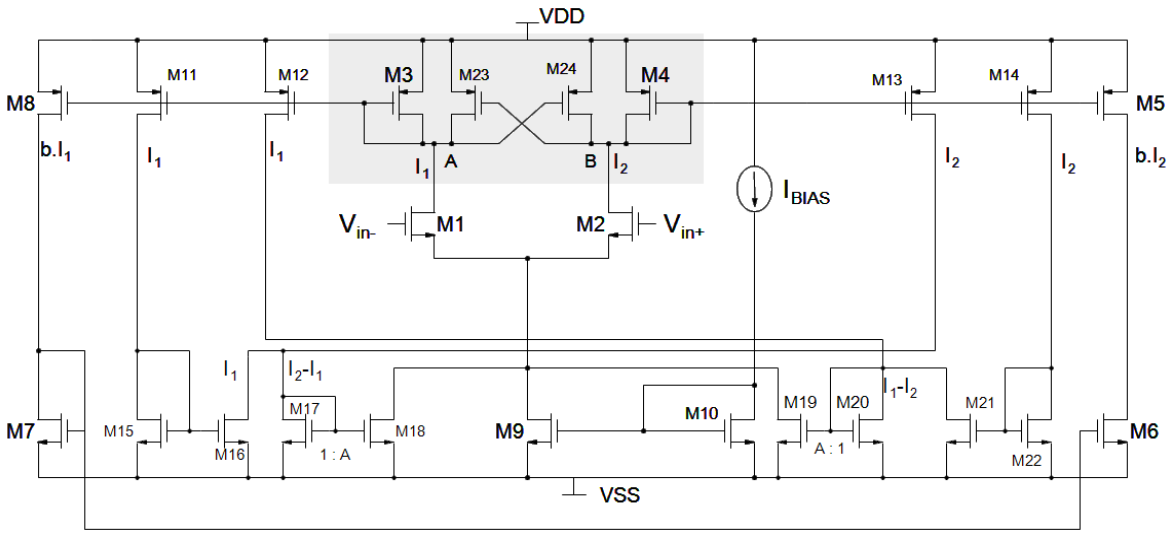

Figure 4-15 Two stage OTA with adaptive bias circuit and gain enhancement circuit [5]

The load transistor of the in Figure 4-14 is a diode connected load, hence the output resistance of load is very small. The shaded region shown in the Figure 4-15 is a compensator circuit used to increase the DC gain. By adding the extra circuit the trance conductance of the overall load is becoming $g_{m4} - g_{m23}$, which increases the gain of the first stage as well as the overall gain.

4.2.1 Simulation results of Op-amp with current subtractor adaptive bias topology

The simulation of sub-threshold Op-amp with current subtractor adaptive bias topology has been done using UMC 180 nm technology with supply voltage of ± 0.6 V. The current source shown in the Figure 4-15 is replaced by a transistor with a bias voltage.

The Figure 4-16 shows gain, UGB and phase margin are 51.1dB, 4.322MHz and 57.70° respectively.

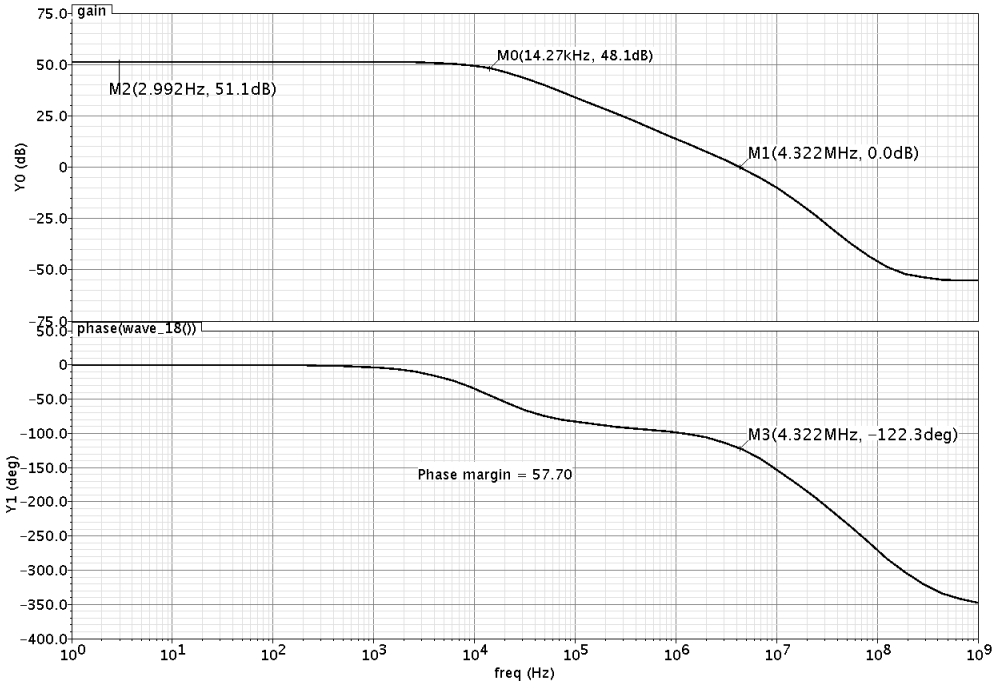

Figure 4-16 Gain and Phase plot of Op-amp with subtractor adaptive bias circuit

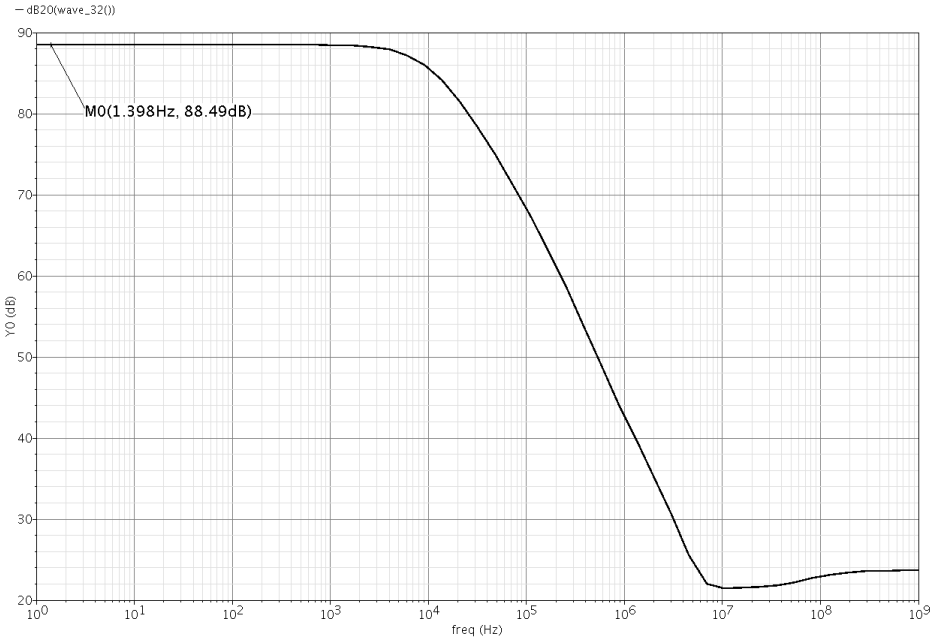

Figure 4-17 CMRR of Op-amp with subtractor adaptive bias circuit

The CMRR of the Op-amp is 88.49dB as shown in the Figure 4-17. The PSRR of this Op-amp is 80.23dB. This Op-amp consumes 1.39uW of power. The SR and the settling

time of the Op-amp is found out by applying a step signal the unit gain configuration and the output is shown in the Figure 4-18. The SR is 4V/us and the settling time is 0.871us.

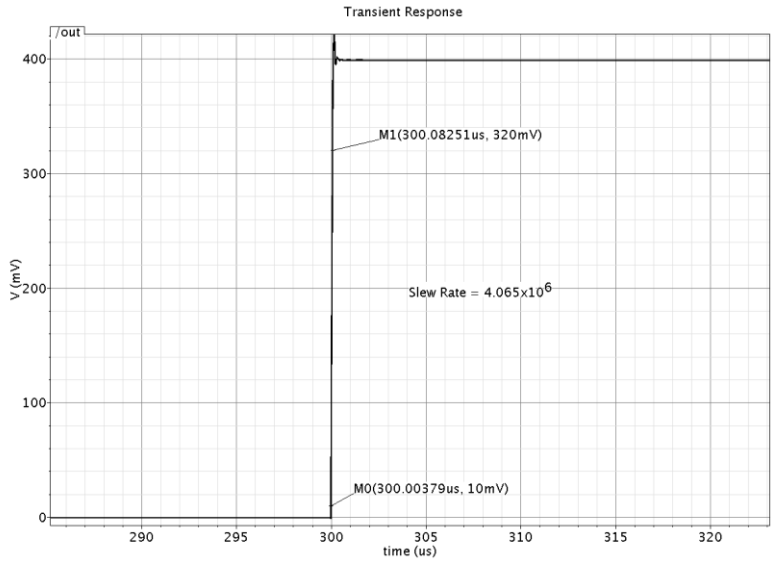

Figure 4-18 Slew Rate of Op-amp with subtractor adaptive bias circuit

The layout of the circuit is shown in Figure 5-4 and the post layout simulation result is tabulated in Table 6.

Table 6: Simulation Results of sub-threshold Op-amp with subtractor adaptive bias circuit

Parameters	**Schematic simulation result**	**Post layout simulation Result**
DC Gain	51.1dB	51.1dB
CMRR	88.49dB	88.47dB
PSRR	80.23dB	80.23dB
UGB	4.322MHz	4.524MHz
SR	4.065V/us	3.41V/us
Phase margin	57.70°	63.20°
Settling time	0.871us	0.909us
Power	1.39uW	1.42uW

4.3 Simulation result comparison of different architecture of op-amp

In this thesis, we discussed about four different type Op-amp circuit, in this section we will show the comparison of these four Op-amp performances.

All four Op-amp circuit simulation has been done in UMC 180nm technology with BISM 3v3 level 11 model, the simulation results of schematic and av-extracted view has been presented in previous sections. The performance comparison of all four Op-amp structure is presented in the Table 7.

Table 7: Comparison of Op-amp performances

PARAMETERS	Conventional	Sub-threshold	With WTA circuit based adaptive biased circuit	With subtractor based adaptive bias circuit
SUPPLY VOLTAGE	1.8V	0.8V	0.8V	$\pm$0.6V
DC gain	64.37dB	67.79 dB	67.67 dB	51.1 dB
UGB	25.55MHz	1.224 MHz	1.325 MHz	4.322 MHz
SR	26.4$V/\mu s$	0.311 $V/\mu s$	1.63$V/\mu s$	4.065 $V/\mu s$
CMRR	68.37dB	56.91 dB	81.45 dB	88.49 dB
PSRR	72.63 dB	34.51 dB	34.0 dB	80.23 dB
SETTLING TIME	91.035 ns	5.28 μs	4.66 μs	0.909 μs
POWER	276.8 μW	0.830 μW	1.0027 μW	1.39 μW
PHASE MARGIN	64.19°	63.60°	58.1°	57.7°
OPERATION MODE	Saturation	Sub-threshold	Sub-threshold	Sub-threshold

The basic objective of this work was to reduce the power of an Op-amp with a desirable SR value. From the above table we can observe that a conventional Op-amp working in saturation region gives a good frequency response, desirable DC gain, CMRR, PSRR, system stability and very high slew rate. But this Op-amp is very power hungry circuit,

which contradicts our objective of Op-amp design. For reducing the power of the Op-amp we preferred to go for an Op-amp operating in sub-threshold region. While, working with sub-threshold region it reduces the power of the circuit as per our requirement, but, it reduces the slew rate and increases the settling time with a descent phase margin. The reduction of slew rate is needs to be improved, for that we used the adaptive bias circuit. We examined two adaptive bias techniques(WTA, subtractor) and the results are presented. The Op-amp using WTA circuit is gives five times higher slew rate than the sub-threshold Op-amp circuit. the power of this Op-amp is little higher than the sub-threshold Op-amp. The gain and phase margin values are almost similar for both Op-amp. The Op-amp circuit with subtractor adaptive biased topology gives a better slew rate value than two above discussed sub-threshold Op-amp circuit. But gain of this Op-amp circuit is lower than the all other Op-amp presented in this thesis.

5

CONCLUSION

An Op-amp operating in sub-threshold region gives the advantage low power over the conventional Op-amp in saturation region, the power required for the conventional Op-amp presented in this thesis is 276μW, but in sub-threshold Op-amp consumes only 0.830 μW of power. As the drain current in sub-threshold region reduced the slew rate of subthreshold Op-amp is reduced from 26.4 $V/\mu s$ to 0.311 $V/\mu s$. For improving the slew rate we have used adaptive biasing technique which increases the biased current of the subthreshold Op-amp under the dynamic condition by keeping the biased current lower for quiescent condition. Two different topology of adaptive biased technique are used. Firstly, adaptive biased using WTA circuit which provides a maximum gate to source voltage difference when difference between the input signal increases. By using this method we achieved a slew rate of 1.63 $V/\mu s$ with a power consumption of 1.0027 μW. This Op-amp gives a decent the DC gain and phase margin. Secondly, adaptive bias circuit using current subtractor circuit, in this technique the bias current is increased by a factor of $1/(1-A)$ (where, A<1) under the dynamic condition. By using this adaptive biased technique the slew rate is increased to 4.065 $V/\mu s$ and the power consumption is becomes 1.39 μW and it gives a better frequency response over WTA adaptive bias technique, but DC gain of this Op-amp is reduced.

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APPENDIX A:

LAYOUTS

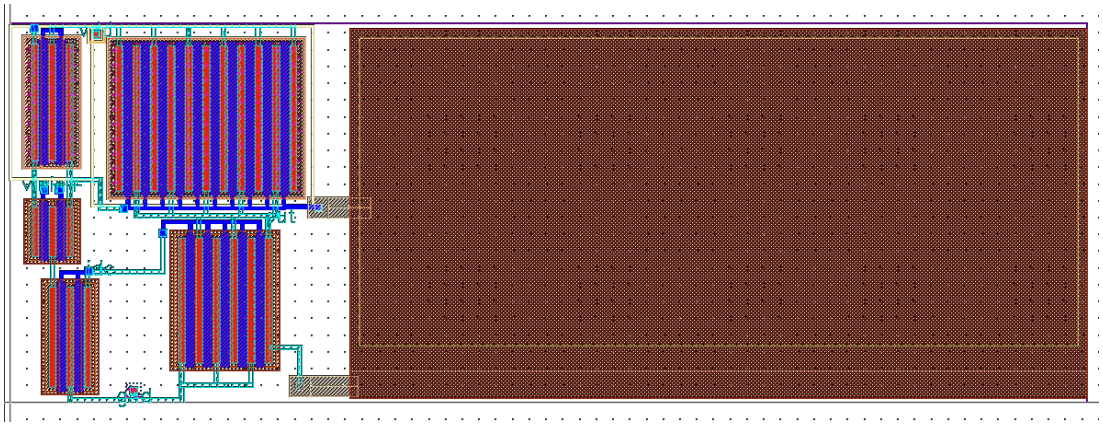

Figure 5-1 Layout of Conventional Op-amp

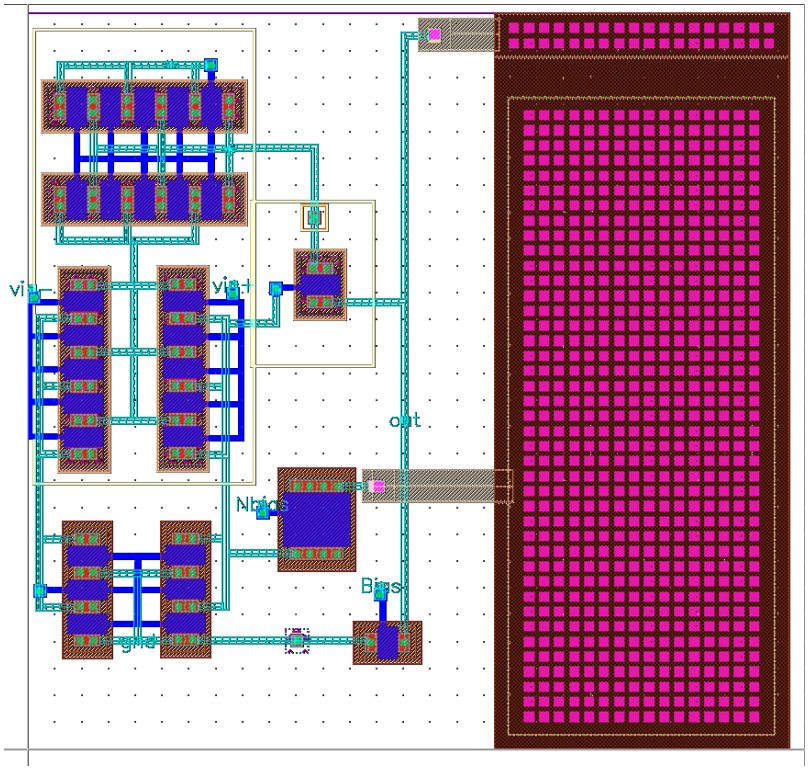

Figure 5-2 Layout of Sub-threshold region Op-amp

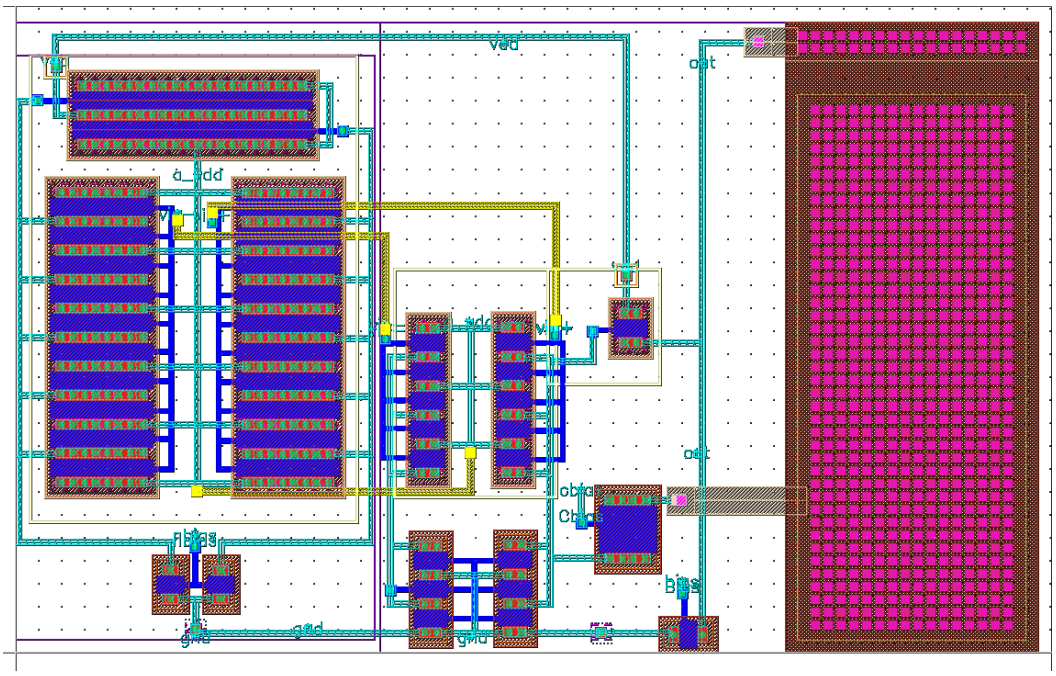

Figure 5-3 Layout of Op-amp with WTA circuit

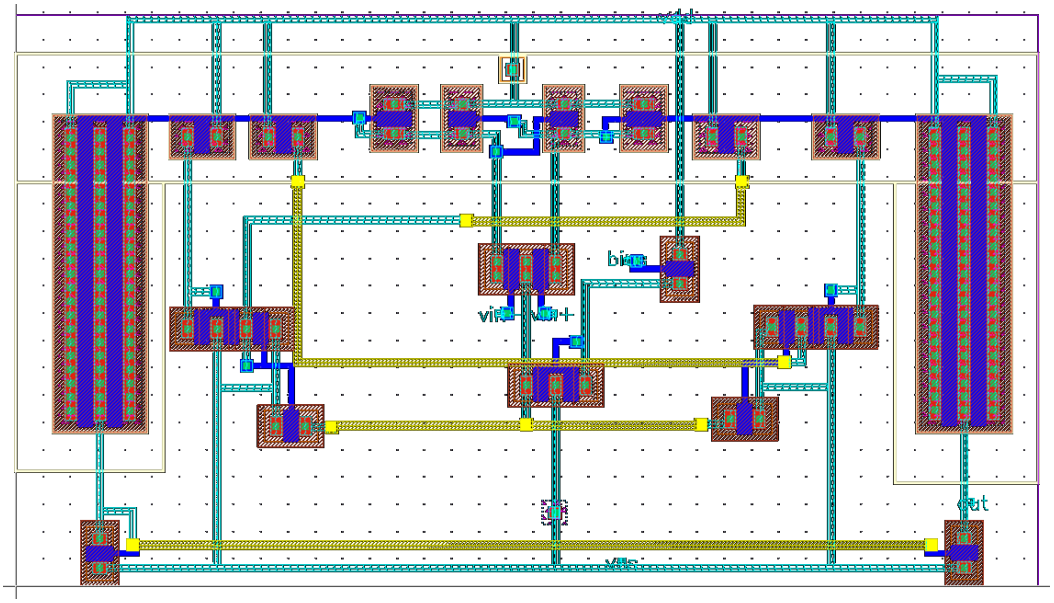

Figure 5-4 Layout of Op-amp with subtractor adaptive bias circuit

APPENDIX B:

W/L RATIO

Table 8: W/L ratio of Conventional Op-amp

Transistor	**W/L**
M1,M2	6
M3,M4	14
M5,M8	12
M6	173
M7	75

Table 9: W/L ratio of Op-amp operating in subthreshold region

Transistor	**W/L**
M1,M2	5/0.72
M3,M4	3/0.72
M5,M8	1.2/0.72
M6	1/0.72
M7	1
M_C	1.2/2

Table 10: W/L ratio of Op-amp with WTA circuit

Transistor	**W/L**
M1,M2	5/0.72
M3,M4	3/0.72
M6	1/0.72
M7, M8, M9	1
M_C	1.2/2
M10, M11	40/0.72
M12,M13	10/0.72

Table 11: W/L ratio of Op-amp with subtractor based adaptive bias circuit

Transistor	**W/L**
M1,M2	1/0.54
M3,M4	0.8/0.54
M5, M8	21.5/0.54
M6, M7	1
M9, M10, M11, M12,	0.72/0.54
M15, M16, M17, M20	0.72/0.54
M18, M19	.7/0.54
M21, M22	0.72/0.54
M23, M24	1